

# An axiomatic basis for computer programming ...on the relaxed Arm-A architecture: the AxSL logic

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# Motivation

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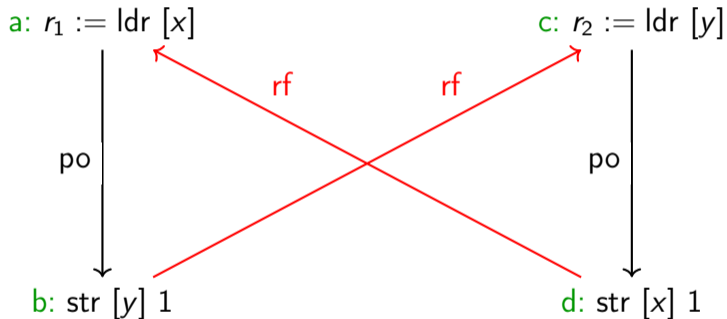
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- We want to reason about programs in weak memory settings, like Arm-A
- We have an authoritative model for user-mode Arm-A
- But we want to reason about programs in a compositional way
- And the Arm-A model is very global

# Why it is hard: Load Buffering



From initial state  $x = y = 0$ , final state  $r_1 = r_2 = 1$  is allowed.

# Incompatibility of simple logics and LB

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Expect both:

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$$\begin{aligned} & \{P * r_1 \mapsto^r v\} \\ & r_1 := \text{ldr } [x] \\ & \{P * r_1 \mapsto^r v'\} \end{aligned}$$

Resources passed between program points

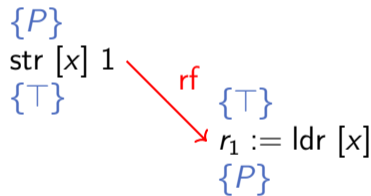


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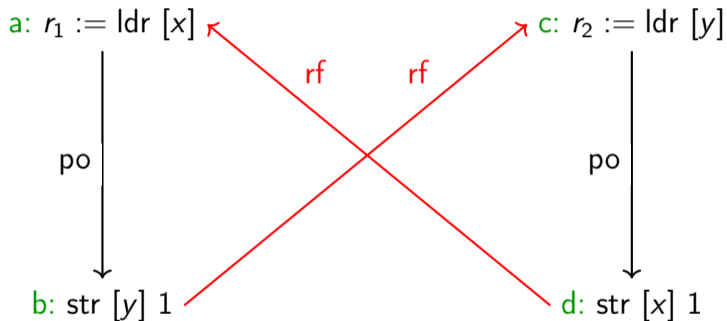
$$\begin{array}{l} \{P * r_1 \mapsto v\} \\ r_1 := \text{ldr } [x] \\ \{P * r_1 \mapsto v'\} \end{array}$$

Resources passed between program points



Resources passed from writes to reads

# Incomptability of simple logics and LB



Logics for RC11 don't suffer this issue as RC11 has  $(\text{po} \cup \text{rf})$  acyclic.

# Existing WM models

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- Operational models
  - Naturally operational
  - Explicit speculation and instruction rewinding

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- Operational models
  - Naturally operational
  - Explicit speculation and instruction rewinding
- Promising models
  - Fairly operational
  - LB requires tricky to reason about certification step
- Axiomatic models
  - Succinct and straightforward to formalise
  - Not at all operational

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- We would like to use the information from the consistency check incrementally as the program executes
- But we cannot easily check consistency of partial executions, because an execution could be made inconsistent by later events



# Opax Semantics

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- Then we incrementally check the guessed graph matches program behaviour

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- Matching an event

$\langle G, F, r := \text{ldr } [a] :: e \rangle \longrightarrow \langle G, F \cup \{R \ a \ v\}, e \rangle$  where  $R \ a \ v \in G \setminus F$

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$$P, Q \in iProp ::= (\text{Iris connectives}) \dots \mid$$
$$r \mapsto v @ a \mid a \wp P \mid \{P\}e\{Q\}_\phi \mid \dots$$

Register value  $v$  comes  
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Register value  $v$  comes from event  $a$        $P$  is tied to event  $a$

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$$P, Q \in iProp ::= (\text{Iris connectives}) \dots \mid$$
$$\underbrace{r \mapsto v@a \mid a \wp P \mid \{P\}e\{Q\}_\phi}_{\text{sound resource passing along po}} \mid \dots$$

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Hoare triple with  
**per-location protocol**  
 $\Phi \in \text{addr} \rightarrow \text{val} \rightarrow \text{eid} \rightarrow iProp$

# Proving MP in AxSL

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a:  $\text{str } [data] \ 42$

b:  $\text{str}_{\text{rel}} [flag] \ 1$

c:  $r_1 := \text{ldr } [flag]$

d:  $r_2 := \text{ldr } [data + r_1 - r_1]$

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a: str [data] 42

↓ po; [Rel] ⊆ ob

b: str<sub>rel</sub> [flag] 1

c: r<sub>1</sub> := ldr [flag]

addr ⊆ ob ↓

d: r<sub>2</sub> := ldr [data + r<sub>1</sub> - r<sub>1</sub>]

# Proving MP in AxSL

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a:  $\text{str} [data] 42$

b:  $\text{str}_{\text{rel}} [flag] 1$

$\{ \dots \}$

$\{ r_1 \mapsto \_ * r_2 \mapsto \_ \}$

c:  $r_1 := \text{ldr} [flag]$

d:  $r_2 := \text{ldr} [data + r_1 - r_1]$

$\left\{ \begin{array}{l} r_1 \mapsto v_{flag} @ \_ * r_2 \mapsto v_{data} @ \_ * \\ (v_{flag} = 1 \Rightarrow v_{data} = 42) \end{array} \right\}$

# Proving MP in AxSL

{ T }

{  $r \mapsto * r \mapsto$  }

a:

The protocol  $\Phi$ :

b:

$$\Phi(data, v, e) \triangleq \text{Initial}(e) \vee v = 42$$

$$\Phi(flag, v, e) \triangleq \text{Initial}(e) \vee (v = 1 * \exists e'. e':W \text{ data } 42 \xrightarrow{po} e:W_{rel} \text{ flag } 1)$$

{

{  $(v_{flag} = 1 \Rightarrow v_{data} = 42)$  }



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a: str [data] 42

{ a:W data 42  $\xrightarrow{\text{po}}$  . }



b: str<sub>rel</sub> [flag] 1      Proof obligation  
                                  $\Phi(\text{data}, 42, a)$

{ ... }

{  $r_1 \mapsto \_ * r_2 \mapsto \_$  }

c:  $r_1 := \text{ldr} [\text{flag}]$

d:  $r_2 := \text{ldr} [\text{data} + r_1 - r_1]$

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a: str [data] 42

{ a:W data 42  $\xrightarrow{\text{po}}$  . }

b: str<sub>rel</sub> [flag] 1

{ a:W data 42  $\xrightarrow{\text{po}}$  b:W<sub>rel</sub> flag 1\* }

{ ... }

Proof obligation  
 $\Phi(\text{flag}, 1, b)$

{  $r_1 \mapsto \_ * r_2 \mapsto \_$  }

c:  $r_1 := \text{ldr} [\text{flag}]$

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c:  $r_1 := \text{ldr } [\text{flag}]$

{ c:R flag  $v_{\text{flag}} \xrightarrow{\text{po}}$  .\*  
 $r_1 \mapsto v_{\text{flag}} @ c * c \not\rightarrow \Phi(\text{flag}, v_{\text{flag}}, c) * \dots$  }

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{ c:R flag  $v_{\text{flag}} \xrightarrow{\text{addr}} d:R \text{ data } v_{\text{data}} *$   
 $r_1 \mapsto v_{\text{flag}} @ c * r_2 \mapsto v_{\text{data}} @ d * c \wp \top *$   
 $d \wp (\Phi(\text{data}, v_{\text{data}}, d) * \Phi(\text{flag}, v_{\text{flag}}, c))$  }

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  - tension between reasoning along program order and induction along ob
- AxSL has an adequacy theorem
  - results proven in AxSL also hold at the meta level w.r.t. the (axiomatic-model-based) Opax semantics
- The statement is similar to standard Iris adequacy, but the proof is novel
  - by **stratification**: two traversals over program executions

# Conclusion

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- AxSL is an expressive program logic for (user-mode) Arm-A memory model, that
  - supports thread-local reasoning and many advanced CSL features
  - is proven sound w.r.t. the axiomatic-model-based Opax semantics (first in Iris)
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- Main limitations
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  - Missing many abstractions
- Our approach will generalise
  - The Opax semantics can be adapted for other axiomatic memory models
  - The resource-tied-to assertions will allow sound reasoning above other very relaxed MMs, e.g. RISC-V

AD: If you like beautiful interactive robots...

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Check out **Glowbot Garden** @ St Mary le Strand Church (3 min away! 12noon-8pm)