

# Multi-core Computing Lecture 3

MADALGO Summer School 2012 Algorithms for Modern Parallel and Distributed Models

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## Multi-core Computing Lectures: Progress-to-date on Key Open Questions

- How to formally model multi-core hierarchies?
- What is the Algorithm Designer's model?
- What runtime task scheduler should be used?
- What are the new algorithmic techniques?
- How do the algorithms perform in practice?



## Lecture 1 & 2 Summary

- Multi-cores: today, future trends, challenges
- Computations & Schedulers
- Cache miss analysis on 2-level parallel hierarchy
- Low-depth, cache-oblivious parallel algorithms

- Modeling the Multicore Hierarchy
- Algorithm Designer's model exposing Hierarchy
- Quest for a Simplified Hierarchy Abstraction
- Algorithm Designer's model abstracting Hierarchy
- Space-Bounded Schedulers



## **Lecture 3 Outline**

- Cilk++
- Internally-Deterministic Algorithms
- Priority-write Primitive
- Work Stealing Beyond Nested Parallelism
- Other Extensions
  - False Sharing
  - Work Stealing under Multiprogramming
- Emerging Memory Technologies



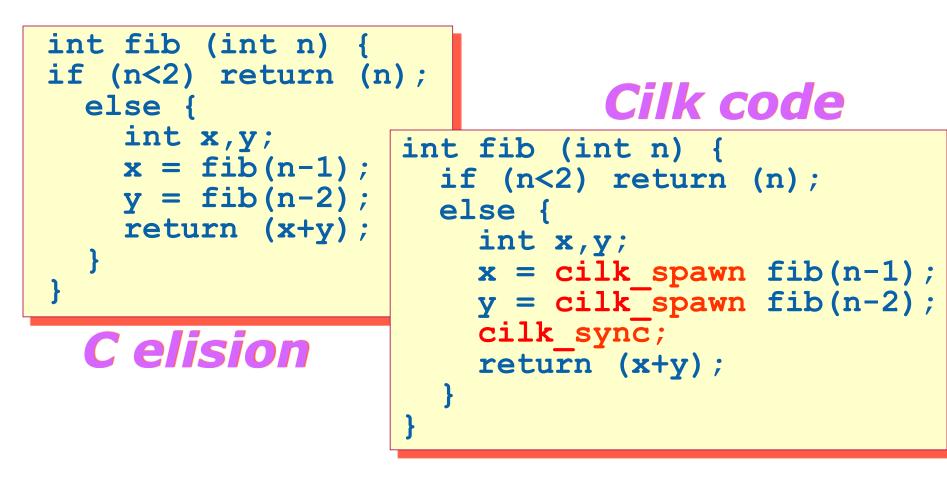
# Multicore Programming using Cilk++

- Cilk extends the C language with just a handful of keywords
- Every Cilk program has a *serial semantics*
- Not only is Cilk fast, it provides *performance guarantees* based on performance abstractions
- Cilk is processor-oblivious
- Cilk's *provably good* runtime system automatically manages low-level aspects of parallel execution, including protocols, load balancing, and scheduling

#### Intel<sup>®</sup> Cilk<sup>™</sup> Plus



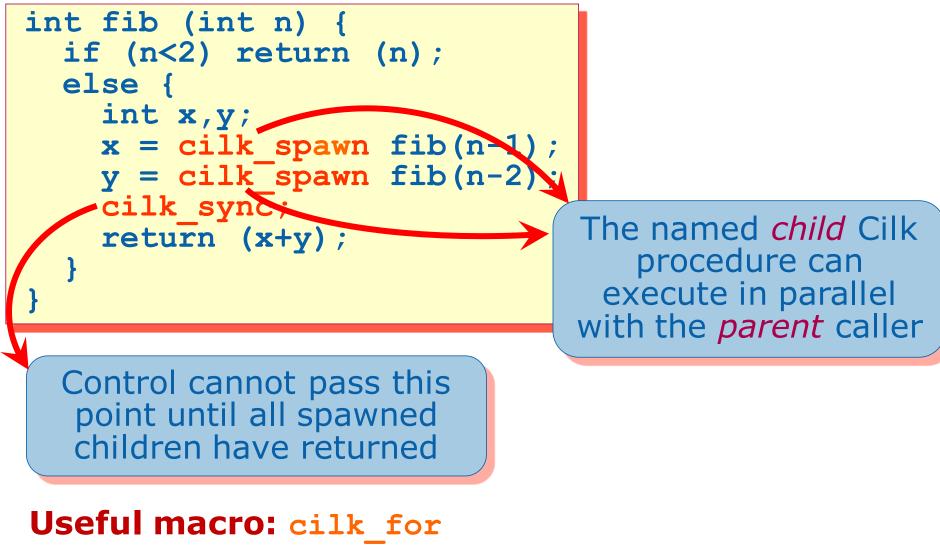
## Cilk++ Example: Fibonacci



Cilk is a *faithful* extension of C. A Cilk program's *serial elision* is always a legal implementation of Cilk semantics. Cilk provides *no* new data types.

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### **Basic Cilk++ Keywords**



for recursive spawning of parallel loop iterates

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## **Nondeterminism in Cilk**

- Cilk encapsulates the nondeterminism of scheduling, allowing average programmers to write deterministic parallel codes using only 3 keywords to indicate logical parallelism
- The Cilkscreen race detector offers provable guarantees of determinism by certifying the absence of determinacy races
- Cilk's reducer hyperobjects encapsulate the nondeterminism of updates to nonlocal variables, yielding deterministic behavior for parallel updates
   See next slide



## Summing Numbers in an Array using sum\_reducer [Frigo et al. '09]

```
int compute(const X& v);
int cilk_main()
Ł
  const std::size_t n = 1000000;
  extern X myArray[n];
  // ...
  sum_reducer <int > result(0);
  cilk_for (std::size_t i = 0; i < n; ++i)
    result += compute(myArray[i]);
  std::cout << "The result is: "
            << result.get_value()
            << std::endl;
  return 0;
```

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## Nondeterminism



#### •Concerned about nondeterminism due to parallel scheduling orders and concurrency



## Nondeterminism is problematic

- Debugging is painful
- Hard to reason
   about code
- Formal verification is hard
- Hard to measure performance

"Insanity: doing the same thing over and over again and expecting different results." - Albert Einstein







# **Inherently Deterministic Problems**

Breadth first search	Spanning forest
Suffix array	Minimum spanning forest
Remove duplicates	Maximal Independent set
Comparison sort	K-nearest neighbors
N-body	Triangle ray intersect
Delaunay triangulation	Delaunay refinement

• Wide coverage of real-world non-numeric problems

• Random numbers can be deterministic



## **External vs. Internal Determinism**

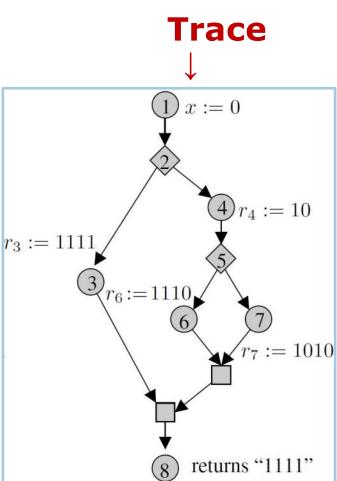
- External: same input  $\rightarrow$  same result
- Internal: same input → same intermediate states
   & same result



### Internal Determinism [Netzer, Miller '92]

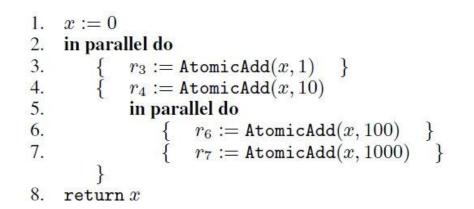
• <u>Trace</u>: a computation's final state, intermediate states, and control-flow DAG

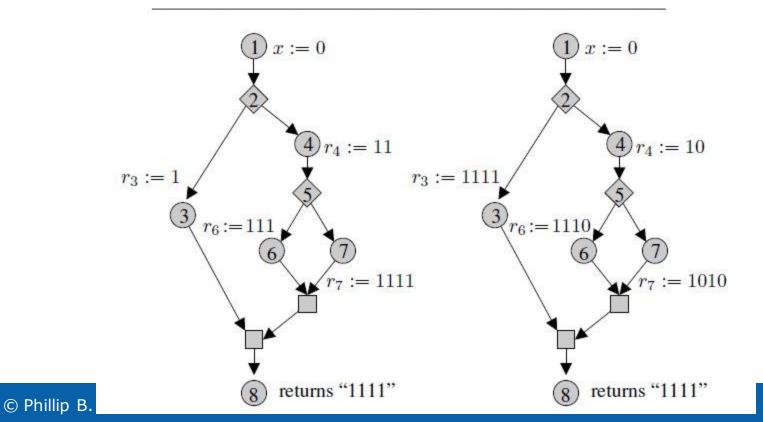
- <u>Internally deterministic</u>: for any fixed input, all possible executions result in equivalent traces (w.r.t. some level of abstraction)
  - Also implies external determinism
  - Provides sequential semantics





# **Internally deterministic?**





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# Commutative + Nested Parallel → Internal Determinism

[Steele '90]

#### Commutativity

- [Steele '90] define it in terms of memory operations
- [Cheng et al. '98] extend it to critical regions
- Two operations f and g commute if f 

   g and g 
   f have same final state and same return values
- We look at commutativity in terms of arbitrary abstraction by introducing "commutative building blocks"
- We use commutativity strictly to get deterministic behavior, but there are other uses...



## **System Approaches to Determinism**

#### **Determinism via**

- Hardware mechanisms [Devietti et al. '11, Hower et al. '11]
- Runtime systems and compilers [Bergan et al. '10, Berger et al. '09, Olszewski et al. '09, Yu and Narayanasamy '09]
- **Operating systems** [Bergan et al. '10]
- Programming languages/frameworks [Bocchino et al. '09]



## **Commutative Building Blocks**

[Blelloch, Fineman, G, Shun '12]

#### Priority write

- pwrite, read
- Priority reserve
  - reserve, check, checkReset
- Dynamic map
  - insert, delete, elements

### • Disjoint set

- find, link

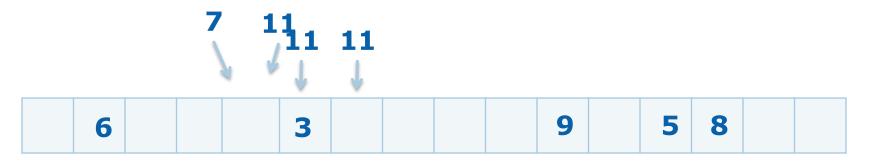
#### • At this level of abstraction, reads commute with reads & updates commute with updates

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# **Dynamic Map**

#### **Using hashing:**

- Based on generic hash and comparison
- Problem: representation can depend on ordering. Also on which redundant element is kept.
- Solution: Use history independent hash table based on linear probing...once done inserting, representation is independent of order of insertion

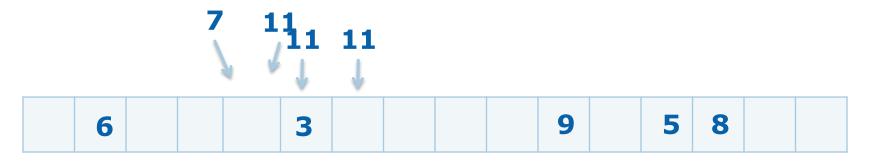


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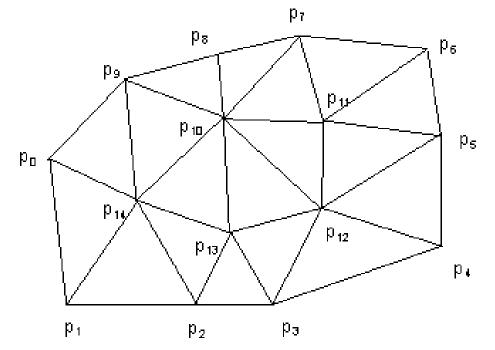
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# **Internally Deterministic Problems**

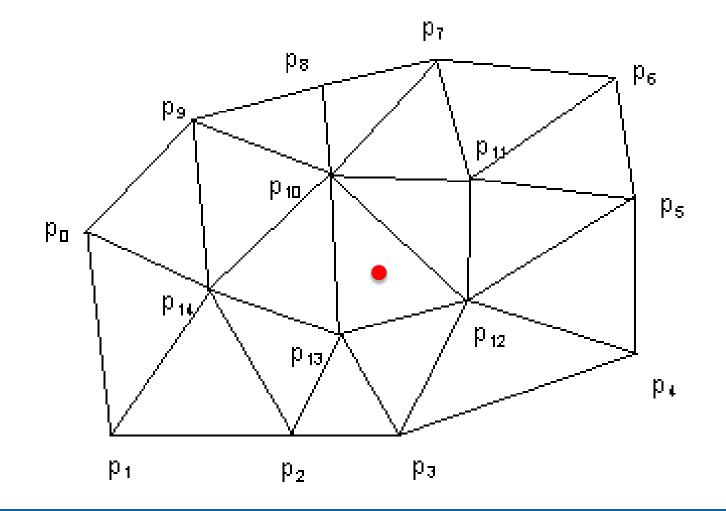
Functional programming	History-independ. data structures	Deterministic reservations			
Suffix array	Remove duplicates	Spanning forest			
Comparison sort	Delaunay refinement	Minimum spanning forest			
N-body		Maximal independent set			
K-nearest neighbors		Breadth first search			
Triangle ray intersed		Delaunay triangulation			
		Delaunay refinement			



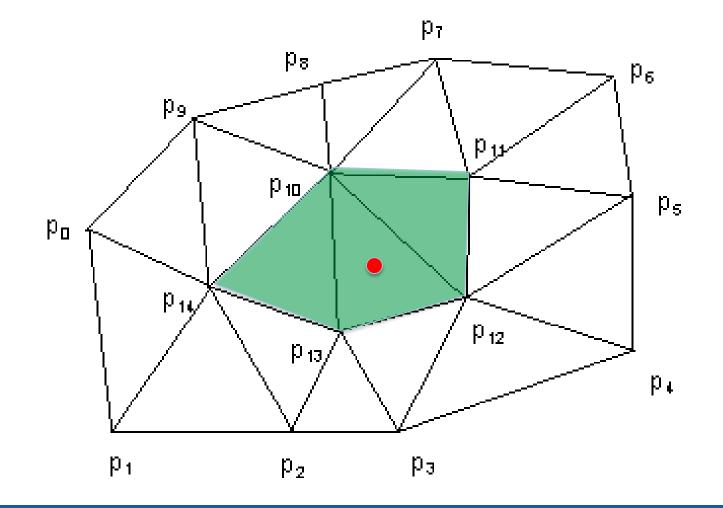
- Incremental algorithm adds one point at a time, but points can be added in parallel if they don't interact
- The problem is that the output will depend on the order they are added.



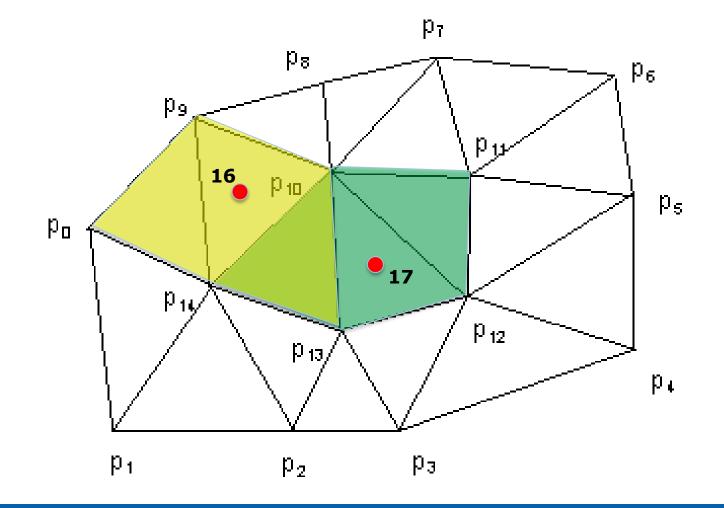
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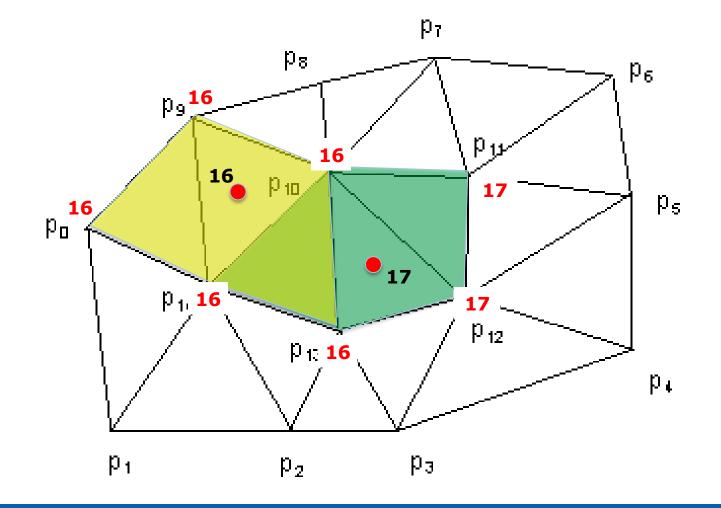




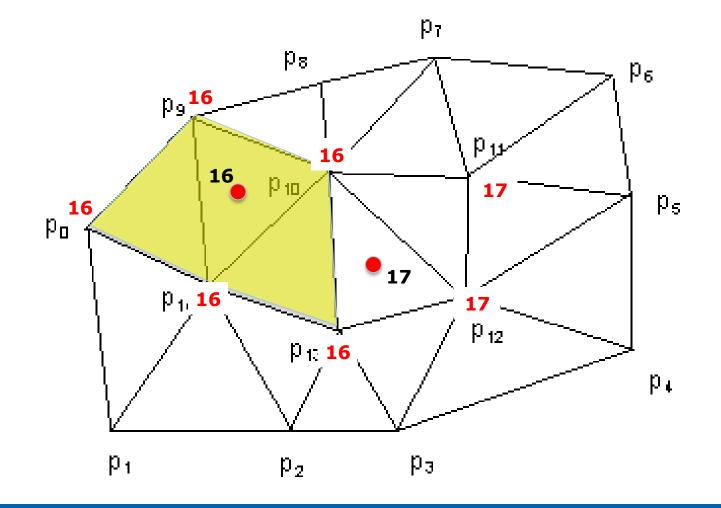














# **Deterministic Reservations**

#### **Generic framework**

iterates = [1,...,n];
while(iterates remain){

Phase 1: in parallel, all i in iterates call reserve(i);

Phase 2: in parallel, all i in iterates call commit(i);

Remove committed i's from iterates;

Note: Performance can be improved by processing prefixes of iterates in each round

#### **Delaunay triangulation/refinement**

```
reserve(i){
    find cavity;
    reserve points in cavity;
}
```

```
commit(i){
    check reservations;
    if(all reservations successful){
        add point and triangulate;
    }
```



}

## **Internally Deterministic Code**

#### • Implementations of benchmark problems

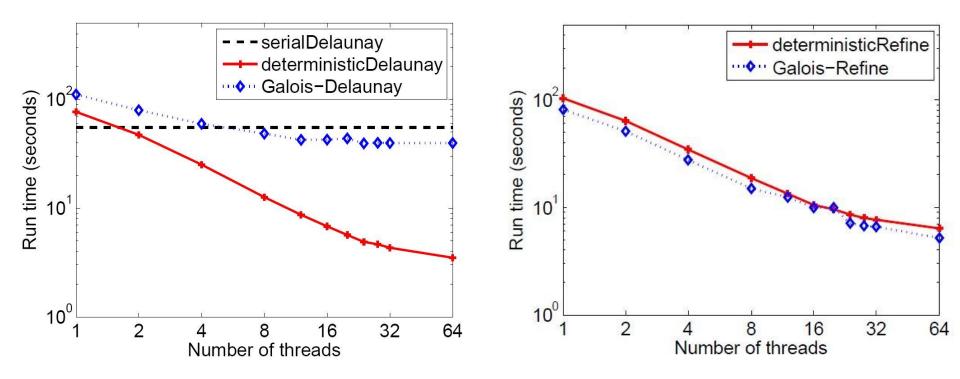
- Internally deterministic
- Nondeterministic
- Sequential
- All require only 20-500 lines of code
- Use nested data parallelism
- Used library of parallel operations on sequences: reduce, prefix sum, filter, etc.



## **Experimental Results**

#### **Delaunay Triangulation**

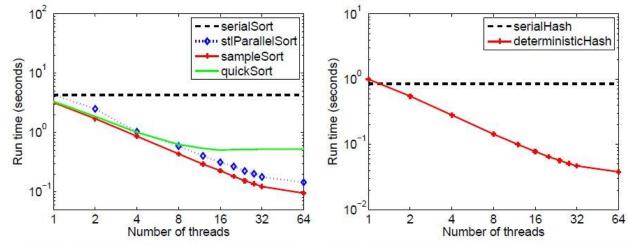
#### **Delaunay Refinement**

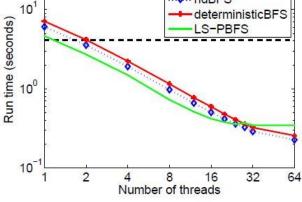


**32-core Intel Xeon 7500 Multicore** Input Sets: 2M random points within a unit circle & 2M random 2D points from the Kuzmin distribution



## **Experimental Results**





-serialBFS

ndBFS

(a) comparison sorting algorithms with a trigram string of length  $10^7\,$ 

(b) remove duplicates algorithms with a trigram string of length  $10^7$ 

(c) BFS algorithms with a random local graph  $(n = 10^7, m = 5 \times 10^7)$ 

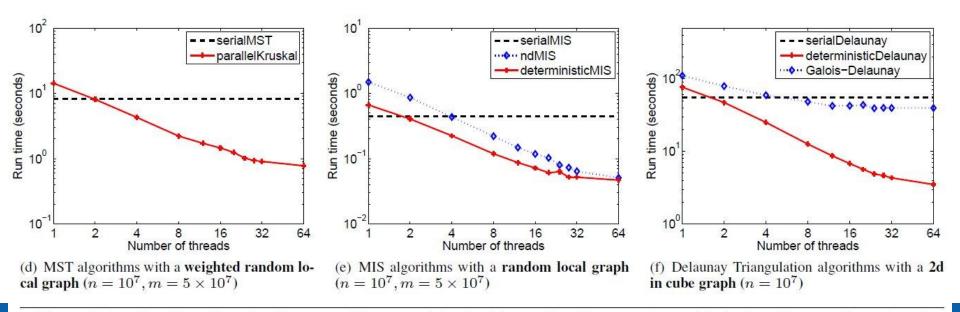


Figure 7. Log-log plots of running times on a 32-core machine (with hyper-threading). Our deterministic algorithms are shown in red.

## Speedups on 40-core Xeon E7-8870

1 12 12		40	CTL ACTL	an an		-	40	(T) (C)	CT1 (CT1
Application Algorithm	thread	40 core	$T_1/T_{40}$	$T_{S}/T_{40}$	Application Algorithm	thread	40 core	$T_{1}/T_{40}$	$T_{S}/T_{40}$
Integer Sort serialRadix Sort parallelRadix Sort	0.48 0.299	0.013	23.0	36.9	Maximal ind. Set serialMIS paralle1MIS	0.405 0.733	0.047	14.1	8.27
Comparison Sort serialSort sampleSort	2.85 2.59	0.066	39.2	43.2	Maximal Matching serialMatching parallelMatching	0.84 2.02	0.108	18.7	7.78
Remove Duplicates seriatHash paratletHash	0.689 0.867	0.027	32.1	25.5	K-Nearest Neighbors octTreeNeighbors	24.9	1.16	21.5	-
Dictionary seria1Hash paralle1Hash	0.574 0.748	0.025	29.9	23	Delaunay Triangulation serialDelaunay paralle1Delaunay	56.3 76.6	2.6	29.5	21.7
Breadth First Search seria1BFS paralle1BFS	2.61 5.54	0.247	22.4	10.6	Convex Hull seriatHull quickHutt	1.01 1.655	0.093	17.8	10.9
Spanning Forest serialSF parallelSF	1.733 5.12	0.254	20.1	6.81	Suffix A rray serialKS parallelKS	17.3 11.7	0.57	20.5	30.4
Min Spanning Forest seria1MSF paralle1Kruskal	7.04 14.9	0.626	23.8	11.2	Ray Casting kdTree	7.32	0.334	21.9	-



### Problem Based Benchmark Suite http://www.cs.cmu.edu/~pbbs/

- **Goal: A set of "problem based benchmarks"** Must satisfy a particular input-output interface, but there are no rules on the techniques used
- Measure the quality of solutions based on:
- Performance and speedup over a variety of input types and w.r.t. best sequential implementations
- Quality of output. Some benchmarks don't have a right answer or are approximations
- Complexity of code. Lines of code & other measures
- Determinism. The code should always return the same output on same input
- Generic. Code should be generic over types
- Correctness guarantees
- Easily analyze performance, at least approximately



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### **Priority Write as a Parallel Primitive** [Shun, Blelloch, Fineman, G]

- **<u>Priority-write</u>**: when there are multiple writes to a location, possibly concurrently, the value with the highest priority is written
  - E.g., write-with-min: for each location, min value written wins (used earlier in Delaunay Refinement)

A := 5 B := 17 B := 12 A := 9 A := 8 yields A = 5 and B = 12

#### Useful parallel primitive:

- + Low contention even under high degrees of sharing
- + Avoids many concurrency bugs since commutes
- + Useful for many algorithms & data structures



#### **Priority-Write Performance**

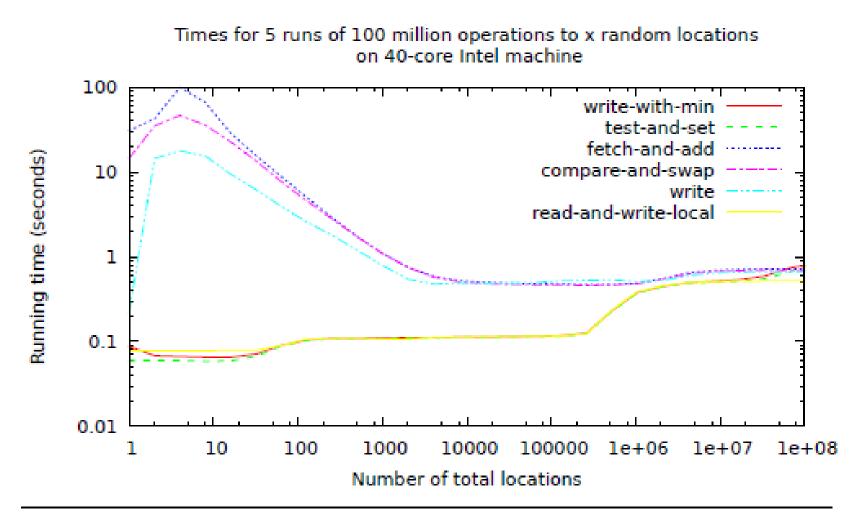


Figure 1. Time for six different operations types on a 40-core Intel Nehalem under various degrees of sharing (log-log scale).

#### c Similar results on 48-core AMD Opteron 6168

### **Theoretical Justification**

Lemma: Consider a collection of n distinct prioritywrite operations to a single location, where at most p randomly selected operations occur concurrently at any time. Then the number of CAS attempts is O(p In n) with high probability.

Idea: Let X\_k be an indicator for the event that the kth priority-write performs an update. Then X\_k = 1 with probability 1/k, as it updates only if it is the highest-priority of all k earliest writes. The expected number of updates is then given by  $E[X_1+...+X_n] = 1/1+1/2+1/3+...+1/n = H_n$ .



# **Priority-Write in Algorithms**

- Take the maximum/minimum of set of values
- Avoiding nondeterminism since commutative
- Guarantee progress in algorithm: highest priority thread will always succeed
- Deterministic Reservations: speculative parallel FOR loop (use iteration as priority)

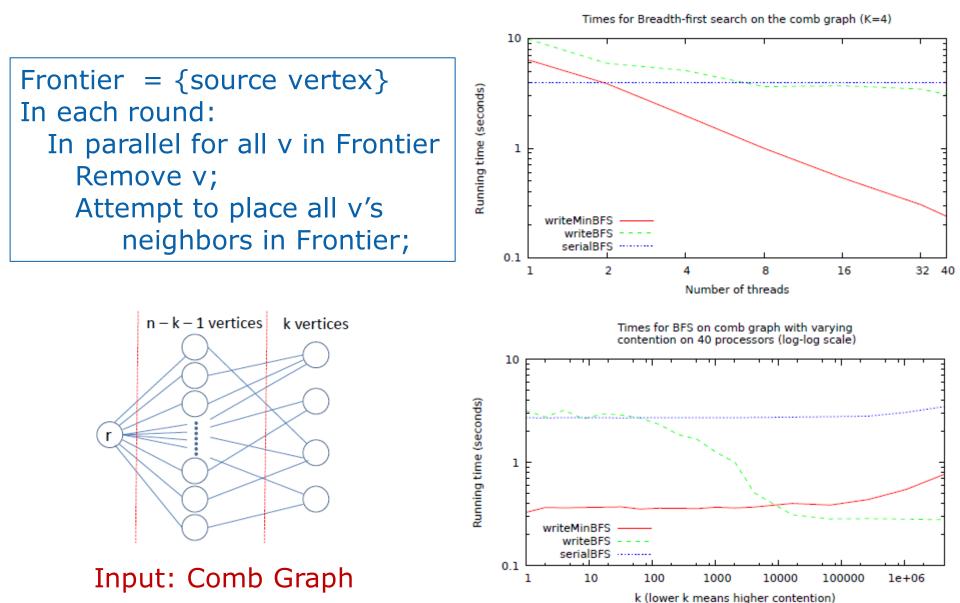


## **Priority Writes in Algorithms**

- Parallel version of Kruskal's minimum spanningtree algorithm so that the minimum-weight edge into a vertex is always selected
- Boruvka's algorithm to select the minimumweight edge
- Bellman-Ford shortest paths to update the neighbors of a vertex with the potentially shorter path
- Deterministic Breadth-First Search Tree



## E.g., Breadth-First Search Tree



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## **Priority-Write Definition**

```
procedure PRIORITYWRITE(addr, newval, comp)
   oldval \leftarrow *addr
   while comp(newval, oldval) do
       if CAS(addr, oldval, newval) then
           return
       else
           oldval \leftarrow *addr
       end if
   end while
end procedure
```

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#### **Priority-Writes on Locations**

- Efficient implementation of a more general dictionary-based priority-write where the writes/inserts are made based on keys.
  - E.g., all writers might insert a character string into a dictionary with an associated priority
  - Use for prioritized remove-duplicates algorithm

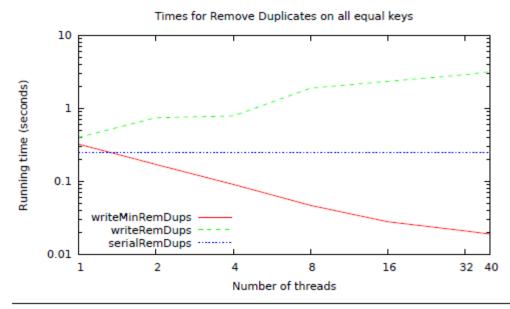
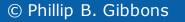


Figure 9. Remove Duplicates times on the allEqual sequence (log-log scale)





### **Lecture 3 Outline**

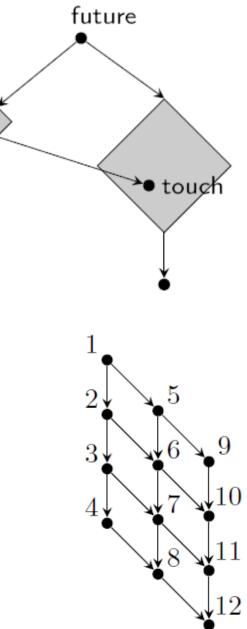
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# **Parallel Futures**

- Futures [Halstead '85], in Multilisp
  - Parallelism no longer nested
  - Here: explicit future and touch keywords
  - E.g. Halstead's quicksort, pipelining tree merge [Blelloch, Reid-Miller '97]

- Strictly more expressive than fork/join
  - E.g. can express parallel pipelining
- ... but still deterministic!



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## **Work Stealing for Futures?**

- Implementation choices:
  - What to do when touch causes processor to stall?

- Previous work beyond nested parallelism:
  - Bound # of steals for WS [Arora et al. '98]
  - We show: not sufficient to bound WS overhead, once add futures!

#### **Summary of previous work**

Nested Parallelism: O(Pd) steals, Overheads additive in # of steals Beyond Nested Parallelism: O(Pd) steals, # steals can't bound overheads



future

≯● tou¢

### **Bounds for Work Stealing with Futures**

[Spoonhower, Blelloch, G, Harper '09]

Extend study of Work Stealing (WS) to Futures:

- Study "deviations" as a replacement for "steals"
  - Classification of deviations arising with futures
  - Tight bounds on WS overheads as function of # of deviations
- Give tight upper & lower bounds on # of deviations for WS  $\Theta(Pd + Td)$ , where T is # of touches
- Characterize a class of programs using futures effectively
  - Only O(Pd) deviations

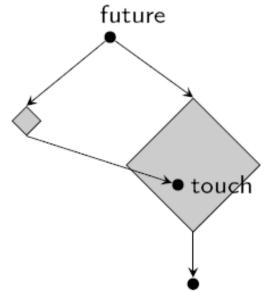
### Futures + Parallelism

#### Processor can stall when:

- 1. No more tasks in local work queue
- 2. Current task is waiting for a value computed by another processor

#### Existing WS only steals in case 1

- We call these *parsimonious* schedulers (i.e., pays the cost of a steal only when it must)
- Thus, in case 2, stalled processor jumps to other work on its local work queue





## Deviations

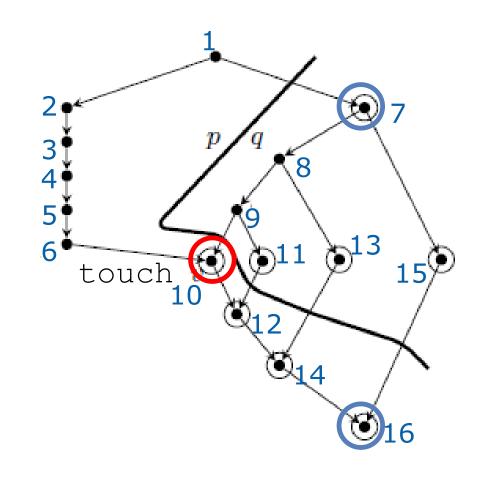
- A deviation (from the sequential schedule) occurs when...
  - a processor p visits a node n,
  - the sequential schedule visits n' immediately before n
  - ...but *p* did not.
- Used by [Acar, Blelloch, Blumofe '02] to bound additional cache misses in nested parallelism
- Our work: use deviations as means to bound several measures of performance
  - Bound # of "slow clone" invocations (≈ computation overhead)
  - Bound # of cache misses in private LRU cache



## **Sources of Deviations**

- In nested parallelism:
  - at steals & joins
  - # deviations ≤ 2× # steals

- With futures:
  - at steals & joins
  - at touches
  - indirectly after touches (rest)





### **Bounding WS Overheads**

 $\Delta = #$  of deviations

#### **Invocations of slow clones**

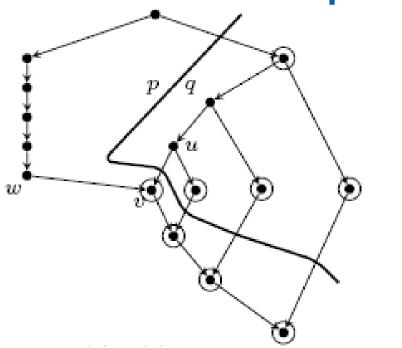
- Theorem: # of slow clone invocations  $\leq \Delta$
- Lower bound: # of slow clone invocations is  $\Omega(\Delta)$

Cache misses (extension of [Acar, Blelloch, Blumofe '02])

- Theorem: # of cache misses  $< Q_1(M) + M \Delta$ 
  - Each processor has own LRU cache; under dag consistency
  - M = size of a (private) cache
  - Q<sub>1</sub>(M) = # of cache misses in sequential execution

## **Deviations: Example Graphs**

2 processors: p & q



1 future, 1 touch, 1 steal, span=d

#### Ω(d) deviations

T futures, T touches, 1 steal, O(log T) span

**Ω(T)** deviations

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Bounding Deviations, Upper Bound Main Theorem:

∀ computations derived from futures with depth d and T touches, the expected # deviations by any parsimonious WS scheduler on P processors is O(Pd + Td)

- First term O(Pd) based on previous bound on # of steals
- Second term O(Td) from indirect deviations after touches

#### **Proof relies on:**

- Structure of graphs derived from uses of futures
- Behavior of parsimonious WS



### **Pure Linear Pipelining**

- Identified restricted use case w/ less overhead
  - . # of deviations is O(Pd)
- Includes producer-consumer examples with streams, lists, one-dimensional arrays



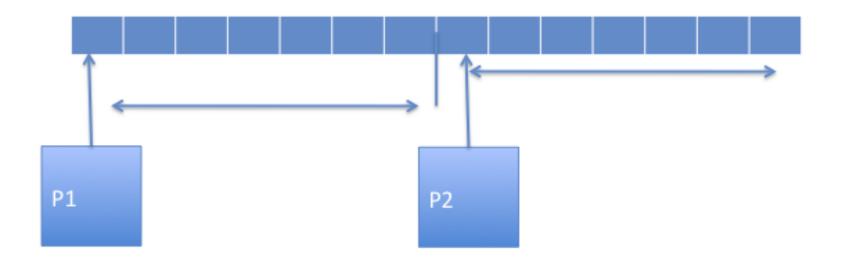
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#### **False Sharing**

Block of size B shared by P1 and P2



False Sharing: B/2 cache misses incurred by P1 and by P2



## **Block-Resilience**

[Cole, Ramachandran '12]

 Hierarchical Balanced Parallel (HBP) computations use balanced fork-join trees and build richer computations through sequencing and recursion

 Design HBP with good sequential cache complexity, and good parallelism

• Incorporate block resilience in the algorithm to guarantee low overhead due to false sharing

• Design resource-oblivious algorithms (i.e., with no machine parameters in the algorithms) that are analyzed to perform well (across different schedulers) as a function of the number of parallel tasks generated by the scheduler



#### BOUNDS FOR RANDOMIZED WORK STEALING (RWS)

Block Resilient	RWS Expected # Steals, S	Cache Misses with	FS Misses
HBP Algorithm	with FS Misses [Cole-R12c]	S Steals [Cole-R12a]	[Cole-R12b]
Scans, MT	$p \cdot (\log n + \frac{b}{s}B)$	Q + S [FS06,CR12a]	$S \cdot B$
RM to BI	$p \cdot (\log n + \frac{b}{s}B)$	$Q + S \cdot B$	$S \cdot B$
MM, Strassen	$p \cdot (\log^2 n + \frac{b}{s}B\log n)$	$Q + S^{\frac{1}{3}} \frac{n^2}{B} + S$	$S \cdot B$
Depth-n-MM	$p \cdot (n + \frac{b}{s}n\sqrt{B})$	$Q + S^{\frac{1}{3}} \frac{n^2}{B} + S$ [FS06,CR12a]	$S \cdot B$
I-GEP	$p \cdot (n \cdot \log^2 n + \frac{b}{s}n\sqrt{B})$	$Q + S^{\frac{1}{3}} \frac{n^2}{B} + S$ [FS06,CR12a]	$S \cdot B$
BI to RM for	$p \cdot (\log n + \frac{b}{s}B)$	$Q + S \cdot B + \frac{n^2}{B} \log \log_B n$	$S \cdot B$
MM and FFT			
LCS	$p(1+rac{b}{s})\cdot n^{\log_2 3}$	$Q + n\sqrt{S}/B + S$ [FS06,CR12a]	$S \cdot B$
FFT, sort	$p \cdot (\log n \cdot \log \log n)$	$C_{ m sort} = O(Q + S \cdot B)$	$S \cdot B$
	$+\frac{b}{s}B\log_B n$ )	$+\frac{n}{B}\frac{\log n}{\log[(n\log n)/S]}$	
List Ranking	$p \cdot \log n \cdot \log \log n$	$Q + C_{\text{sort}} \cdot \log n$	$S \cdot B$
	$\cdot (\log n + \frac{b}{s}B)$		



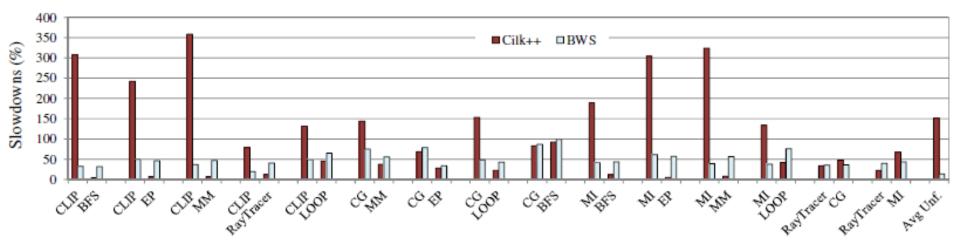
# Multiple Work-Stealing Schedulers at Once?

- Dealing with multi-tenancy
- Want to run at same time
- Schedulers must provide throughput + fairness
  - Failed steal attempts not useful work
  - Yielding at failed steal attempts leads to unfairness
  - BWS [Ding et al. '12] decreases average unfairness from 124% to 20% and increases thruput by 12%

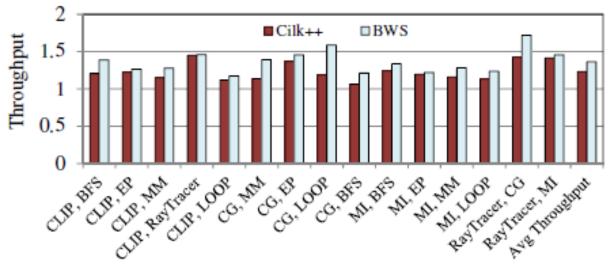
#### Open: What bounds can be proved?



## Unfairness



#### Throughput



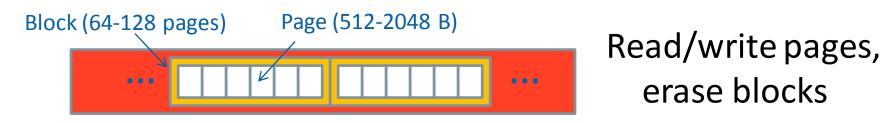
(intel)

### **Lecture 3 Outline**

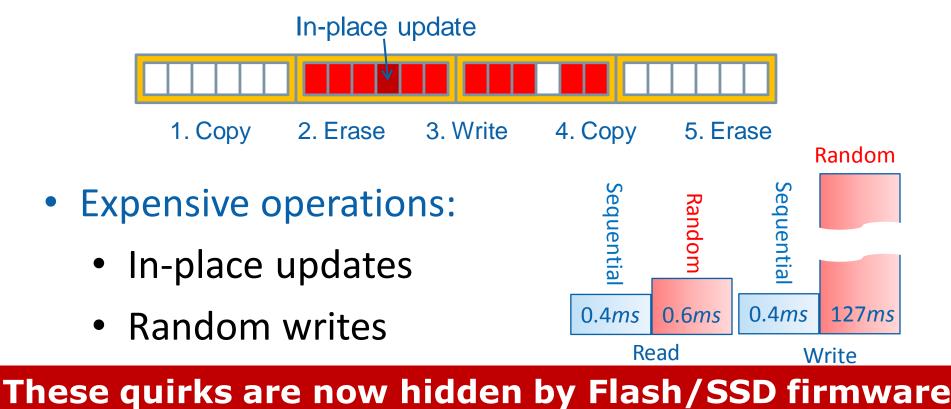
- Cilk++
- Internally-Deterministic Algorithms
- Priority-write Primitive
- Work Stealing Beyond Nested Parallelism
- Other Extensions
  - False Sharing
  - Work Stealing under Multiprogramming
- Emerging Memory Technologies



# **NAND Flash Chip Properties**



Write page once after a block is erased



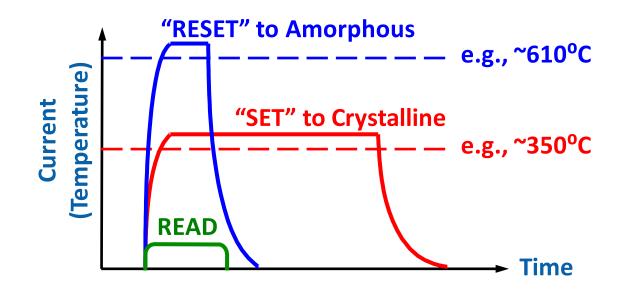
© Phillip B. Gibbons

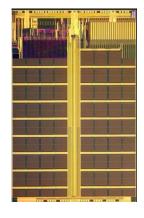
(intel)

# Phase Change Memory (PCM)

- Byte-addressable non-volatile memory
- Two states of phase change material:
  - Amorphous: high resistance, representing "0"
  - Crystalline: low resistance, representing "1"

• Operations:







#### **Comparison of Technologies**

	DRAM	РСМ	NAND Flash
Page size	64B	64B	4KB
Page read latency	20-50ns	~ 50ns	~ 25 μs
Page write latency	20-50ns	~ 1 µs	~ 500 µs
Write bandwidth	~GB/s	50-100 MB/s	5-40 MB/s
	per die	per die	per die
Erase latency	N/A	N/A	~ 2 ms
Endurance	$\sim$	$10^{6} - 10^{8}$	$10^4 - 10^5$
Read energy	0.8 J/GB	1 J/GB	1.5 J/GB [28]
Write energy	1.2 J/GB	6 J/GB	17.5 J/GB [28]
Idle power	~100 mW/GB	~1 mW/GB	1–10 mW/GB
Density	1×	2 – 4×	4×

• Compared to NAND Flash, PCM is byte-addressable, has orders of magnitude lower latency and higher endurance.

Sources: [Doller '09] [Lee et al. '09] [Qureshi et al. '09]

#### **Comparison of Technologies**

	DRAM	PCM	NAND Flash
Page size	64B	64B	4KB
Page read latency	20-50ns	~ 50ns	~ 25 μs
Page write latency	20-50ns	~ 1 µs	~ 500 μs
Write bandwidth	~GB/s	50-100 MB/s	5-40 MB/s
	per die	per die	per die
Erase latency	N/A	N/A	~ 2 ms
Endurance	∞	$10^{6} - 10^{8}$	$10^4 - 10^5$
Read energy	0.8 J/GB	1 J/GB	1.5 J/GB [28]
Write energy	1.2 J/GB	6 J/GB	17.5 J/GB [28]
Idle power	~100 mW/GB	~1 mW/GB	1–10 mW/GB
Density	1×	2 – 4×	4×

• Compared to DRAM, PCM has better density and scalability; PCM has similar read latency but longer write latency

Sources: [Doller '09] [Lee et al. '09] [Qureshi et al. '09]



#### **Relative Latencies:** Read **NAND Flash** Hard Disk DRAM PCM **100ns 10**ns **100us 10ms 10us** 1ms **1us NAND Flash** Hard Disk DRAM PCM Write



#### **Challenge: PCM Writes**

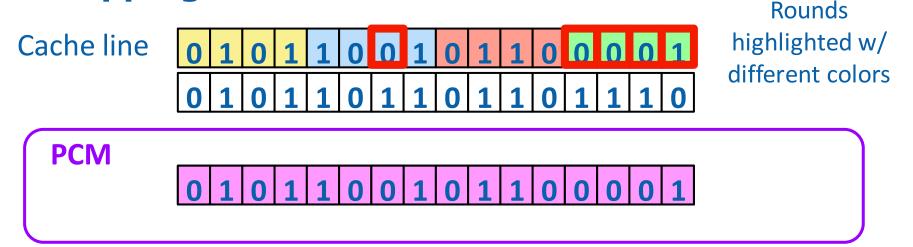
• Limited endurance		PCM
	Page size	64B
<ul> <li>Wear out quickly for</li> </ul>	Page read latency	~ 50ns
hot spots	Page write latency	~ 1 µs
	Write bandwidth	50-100 MB/s
<ul> <li>High energy consumption</li> </ul>		per die
ingi energy consumption	Erase latency	N/A
– 6-10X more energy than	Endurance	$10^{6} - 10^{8}$
a read	Read energy	1 J/GB
	Write energy	6 J/GB
<ul> <li>High latency &amp; low bandwidth</li> </ul>	Idle power	~1 mW/GB
<ul> <li>SET/RESET time &gt; READ time</li> </ul>	Density	2 – 4×

 Limited instantaneous electric current level, requires multiple rounds of writes

## **PCM Write Hardware Optimization**

[Cho, Lee'09] [Lee et al. '09] [Yang et al. '07] [Zhou et al. '09]

- Baseline: several rounds of writes for a cache line
  - Which bits in which rounds are hard wired
- Optimization: data comparison write
  - Goal: write only modified bits rather than entire cache line
  - Approach: read-compare-write
- Skipping rounds with no modified bits



## **PCM-savvy Algorithms?**

#### **New goal: minimize PCM writes**

- Writes use 6X more energy than reads
- Writes 20X slower than reads, lower BW, wear-out

#### **Data comparison writes:**

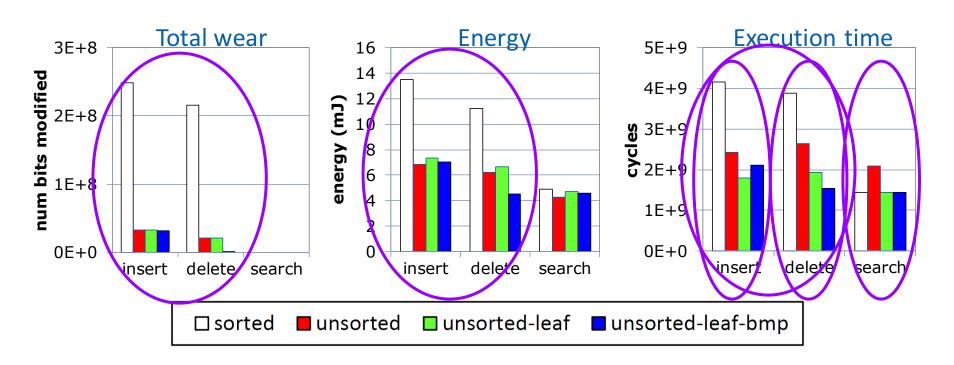
- Minimize Number of bits that change



# **B+-Tree Index**

[Chen, G, Nath '11]

Node size 8 cache lines; 50 million entries, 75% full; Three workloads: Inserting / Deleting / Searching 500K random keys PTLSSim extended with PCM support



#### **Unsorted leaf schemes achieve the best performance**

- For insert intensive: unsorted-leaf
- For insert & delete intensive: unsorted-leaf with bitmap



## Multi-core Computing Lectures: Progress-to-date on Key Open Questions

- How to formally model multi-core hierarchies?
- What is the Algorithm Designer's model?
- What runtime task scheduler should be used?
- What are the new algorithmic techniques?
- How do the algorithms perform in practice?



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