Reasoning About a Machine with Local Capabilities
Provably Safe Stack and Return Pointer Management
Technical Appendix Including Proofs and Details

Lau Skorstengaard  Dominique Devriese
Aarhus University  imec-DistriNet, KU Leuven
lask@cs.au.dk  dominique.devriese@cs.kuleuven.be

Lars Birkedal
Aarhus University
birkedal@cs.au.dk

April 4, 2018

Contents

1 Capability Machine Definition and Operational Semantics 2
  1.1 Domains and Notation .................................................... 2
  1.2 Operational Semantics .................................................. 5

2 Malloc specification ....................................................... 9

3 Macros ............................................................................. 9
  3.1 Linking and ABI ............................................................. 9
  3.2 Flag table .................................................................... 10
  3.3 Macro definitions .......................................................... 10
  3.4 Stack .......................................................................... 15
  3.5 Labels ......................................................................... 21

4 Examples ........................................................................... 25
  4.1 Encapsulation of Local State ............................................. 25
  4.2 Encapsulation of Local State Using Local Capabilities and scall ............................................. 28
  4.3 Well-Bracketedness Using Local Capabilities and scall ....................................................... 32
  4.4 Inverted Control and Return From Closure ................................................................. 38
  4.5 Variant of the “awkward” example ........................................ 38

5 Logical Relation .................................................................. 48
  5.1 Worlds ........................................................................ 48
  5.2 The logical relation ......................................................... 51
  5.3 Useful regions ............................................................... 54
  5.4 Lemmas ........................................................................ 54
    5.4.1 Anti-reduction for the observation relation ................................................................. 54
1 Capability Machine Definition and Operational Semantics

1.1 Domains and Notation

\begin{align*}
\text{Addr} & \triangleq \mathbb{N} \\
\text{Word} & \triangleq \text{Cap} + \mathbb{Z} \\
\text{Reg} & \triangleq \text{RegisterName} \rightarrow \text{Word} \\
\text{Mem} & \triangleq \text{Addr} \rightarrow \text{Word} \\
\text{Perm} & ::= \text{O} \mid \text{RO} \mid \text{RW} \mid \text{RWL} \mid \text{RX} \mid \text{E} \mid \text{RX} \mid \text{RWX} \mid \text{RWLX} \\
\text{ExecConf} & \triangleq \text{Reg} \times \text{Mem} \\
\text{Global} & ::= \text{GLOBAL} \mid \text{LOCAL} \\
\text{Cap} & \triangleq (\text{Perm} \times \text{Global}) \times \text{Addr} \times (\text{Addr} + \{\infty\}) \times \text{Addr} \\
\text{Conf} & \triangleq \text{ExecConf} + \{\text{failed}\} + \{\text{halted}\} \times \text{Mem} \\
\text{MemSegment} & \triangleq \text{Addr} \rightarrow \text{Word}
\end{align*}

Local capabilities have been added by adding a new domain Global which represents whether a capability is local or global. There are two new permissions RWL and RWLX that permits writing local capabilities. They are otherwise the same as their non-“permit write local” counterparts.
As we have $\infty$ as a possible address, but our words cannot express $\infty$. We pick $-42$ as a representative for $\infty$ when it is in memory (we could have picked any negative number). Note that $-42$ is not an address, so for address operations $-42$ only represents $\infty$. It is the responsibility of the programmer to keep track of what represents addresses (and take necessary precautions).

Define the following predicate:

**Definition 1.** We say word $w$ "$w$ is non-local" iff either

- $w = ((\text{perm}, g), \text{base}, \text{end}, a) (\text{perm}, \text{GLOBAL})$ for some $\text{perm}$, $a$, $\text{base}$, and $\text{end}$; or
- $w \in \mathbb{Z}$

![Locality hierarchy](image1.png)

Figure 1: Locality hierarchy

Things to note:

- RegisterName contains pc, but is otherwise a sufficiently large finite set.
- Table 1 describes what all the permissions grant access to.
- Figure 2 shows the ordering of the permissions, i.e., the elements of Perm.
- Figure 3 shows the ordering of LOCAL and GLOBAL, i.e., the elements of Global.
- The ordering of Perm $\times$ Global is pointwise.

![Permission hierarchy](image2.png)

Figure 2: Permission hierarchy
<table>
<thead>
<tr>
<th></th>
<th>Permissions</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>No permissions. Grants no permissions</td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>Read only. Grants read permission</td>
<td></td>
</tr>
<tr>
<td>RW</td>
<td>Read-write. Grants read and write permission. Storage of local capabilities prohibited.</td>
<td></td>
</tr>
<tr>
<td>RWL</td>
<td>Read-write, permit write local. Grants read and write permission. Storage of local capabilities possible.</td>
<td></td>
</tr>
<tr>
<td>RX</td>
<td>Execute permission. Grants execute and read permissions.</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>Enter permission. This permission grants no access, but when jumped to, it will turn into an RX permission.</td>
<td></td>
</tr>
<tr>
<td>RWX</td>
<td>Read-write-execute permission. Grants read, write, and execute permissions. Storage of local capabilities prohibited.</td>
<td></td>
</tr>
<tr>
<td>RWLX</td>
<td>Read-write-execute, permit write local. Grants read, write, and execute permissions. Storage of local capabilities possible.</td>
<td></td>
</tr>
</tbody>
</table>

Table 1: The permissions in this capability system

Notation:

\[
\begin{align*}
i & \in \text{Instructions} \\
r & \in \text{RegisterName} \\
\text{pc} & \in \text{Cap} \\
\text{pc} & \in \text{RegisterName} \\
\Phi & \in \text{ExecConf} \\
m, \Phi, \text{mem} & \in \text{Mem} \\
\Phi, \text{reg} & \in \text{Reg} \\
a & \in \text{Addr} \\
\text{perm} & \in \text{Perm} \\
((\text{perm}, g), \text{base}, \text{end}, a) & \in \text{Cap} \\
n & \in \mathbb{Z} \\
\text{ms} & \in \text{MemSegment} \\
\end{align*}
\]

Words and instructions:

\[
\begin{align*}
lv & ::= [r] \\
hv & ::= ⟨r⟩_m \\
rv & ::= n \mid lv \\
i & ::= \text{jmp} lv \mid \text{jnz} lv lv \mid \text{move} lv rv \mid \text{load} lv hv \mid \text{store} hv rv \mid \\
& \text{plus} lv rv rv \mid \text{minus} lv rv rv \mid \text{lt} lv rv rv \mid \text{lea} lv rv \mid \text{restrict} lv rv \mid \text{subseg} lv rv rv \mid \\
& \text{isptr} lv rv \mid \text{getp} lv lw \mid \text{getl} lv lw \mid \text{getb} lv lw \mid \text{gete} lv lw \mid \text{geta} lv lw \mid \\
& \text{fail} \mid \text{halt} \\
\end{align*}
\]

Further define \(\text{reg}_0 \in \text{Reg}\) such that

\[
\forall r \in \text{RegisterName}. \text{reg}_0(r) = 0
\]
1.2 Operational Semantics

Assume a *decode* function that decodes words to instructions:

\[ \text{decode} : \text{Word} \rightarrow \text{Instructions} \]

Assume an *encodePerm*, *encodeLoc*, and *encodePermPair* function that encodes a permissions, locality, and permission pair, respectively, as an integer:

\[ \text{encodePerm} : \text{Perm} \rightarrow \mathbb{Z} \]
\[ \text{encodeLoc} : \text{Global} \rightarrow \mathbb{Z} \]
\[ \text{encodePermPair} : (\text{Perm} \times \text{Global}) \rightarrow \mathbb{Z} \]

Further, assume a left inverse function, *decodePermPair*, that decodes permissions

\[ \text{decodePermPair} : \mathbb{Z} \rightarrow (\text{Perm} \times \text{Global}) \]

We define the operational semantics as follows:

\[ \Phi \rightarrow [\text{decode}(\Phi.\text{mem}(a))] (\Phi) \quad \text{if} \quad \Phi.\text{reg}(pc) = (\text{perm, g, base, end, a}) \]
\[ \quad \text{and} \quad \text{base} \leq a \leq \text{end} \]
\[ \quad \text{and} \quad \text{perm} \in \{\text{RX, RWX, RWLX}\} \]
\[ \Phi \rightarrow \text{failed} \quad \text{otherwise} \]

A number of functions and predicates used in the definition of \([\_]\) (defined later). Notice all of them are total.

\[ \text{readAllowed(perm)} = \begin{cases} \text{true} & \text{if} \; \text{perm} \in \{\text{RWX, RWLX, RX, RW, RWL, RO}\} \\ \text{false} & \text{otherwise} \end{cases} \]

\[ \text{writeAllowed(perm)} = \begin{cases} \text{true} & \text{if} \; \text{perm} \in \{\text{RWX, RWLX, RW, RWL}\} \\ \text{false} & \text{otherwise} \end{cases} \]

\[ \text{updatePcPerm}(w) = \begin{cases} ((\text{RX, g, base, end, a}) & \text{if} \; w = ((\text{E, g, base, end, a}) \\ w & \text{otherwise} \end{cases} \]

\[ \text{nonZero}(w) = \begin{cases} \text{true} & \text{if} \; w \in \text{Cap or} \; w \in \mathbb{Z} \; \text{and} \; w \neq 0 \\ \text{false} & \text{otherwise} \end{cases} \]

\[ \text{withinBounds}((\_ , \text{base, end, a})) = \begin{cases} \text{true} & \text{if} \; \text{base} \leq a \leq \text{end} \\ \text{false} & \text{otherwise} \end{cases} \]

\[ \text{updatePc}(\Phi) = \begin{cases} \Phi[\text{reg, pc} \mapsto \text{newPc}] & \text{if} \; \Phi.\text{reg}(pc) = ((\text{perm, g, base, end, a}) \\ \text{and newPc} = ((\text{perm, g, base, end, a + 1}) \\ \text{failed} & \text{otherwise} \end{cases} \]
\[
[\text{fail}] (\Phi) = \text{failed}
\]
\[
[\text{halt}] (\Phi) = (\text{halted}, \Phi.\text{mem})
\]
\[
[\text{jmp } lv] (\Phi) = \Phi[\text{reg.pc} \mapsto \text{updatePcPerm}(\Phi.\text{reg}(lv))]
\]
\[
[\text{jnz } lv \text{ rv}] (\Phi) = \begin{cases} 
\Phi[\text{reg.pc} \mapsto \text{updatePcPerm}(\Phi.\text{reg}(lv))] & \text{if } \text{nonZero}(\Phi.\text{reg}(rv)) \\
\text{updatePc}(\Phi) & \text{if not } \text{nonZero}(\Phi.\text{reg}(rv)) \\
\text{failed} & \text{otherwise}
\end{cases}
\]
\[
[\text{load } [r_1] \langle r_2 \rangle_m] (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg.r_1} \mapsto c]) & \text{if either } n = rv \text{ or } rv = [r_2] \text{ and } n = \Phi.\text{reg}(r_2) \\
\text{updatePc}(\Phi[\text{reg.r_1} \mapsto \Phi.\text{reg}(rv)]) & \text{otherwise}
\end{cases}
\]
\[
[\text{move } [r_1] rv] (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg.r_1} \mapsto rv]) & rv \in \mathbb{Z} \\
\text{failed} & \text{otherwise}
\end{cases}
\]
\[
[\text{lea } [r_1] rv] (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg.r_1} \mapsto c]) & \text{if either } n = rv \text{ or } rv = [r_2] \text{ and } n = \Phi.\text{reg}(r_2) \\
\text{failed} & \text{otherwise}
\end{cases}
\]
\[
[\text{restrict } [r] rv] (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg.r} \mapsto c]) & \text{if } \Phi.\text{reg}(r) = (\text{permPair}, \text{base}, \text{end}, a) \\
\text{failed} & \text{otherwise}
\end{cases}
\]
\[\text{[plus} \, r_1 \, rv_1 \, rv_2\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto n_1 + n_2]) & \text{if } i \in \{1, 2\} \quad (n_i = r v_i, \text{or } n_i = \Phi.\text{reg}(r v_i) \\
\text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[minus} \, r_1 \, rv_1 \, rv_2\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto n_1 - n_2]) & \text{if } i \in \{1, 2\} \quad (n_i = r v_i, \text{or } n_i = \Phi.\text{reg}(r v_i) \\
\text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[lt} \, r_1 \, rv_1 \, rv_2\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto 1]) & \text{if } i \in \{1, 2\} \quad n_i = r v_i, \text{or } n_i = \Phi.\text{reg}(r v_i) \quad \text{and } n_1 < n_2 \\
\text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[subseg} \, r \, rv_1 \, rv_2\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto c]) & \text{if } \Phi.\text{reg}(r) = ((\text{perm}, g), \text{base}, \text{end}, a) \quad \text{and } i \in \{1, 2\} \\
& (n_i = r v_i, \text{or } n_i = \Phi.\text{reg}(r v_i) \quad \text{and } n_1 \in N \\
& \text{and } \text{base} \leq n_1 \quad \text{and } n_2 \leq \text{end} \text{ where } n_2 \in N \\
& \text{or } n_2 = -42 \text{ and } \text{end} = \infty \\
& \text{and perm} \neq \emptyset \\
& \text{and } c = ((\text{perm}, g), n_1, n_2, a) \quad \text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[geta} \, r_1 \, [\, r_2\, ]\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto a]) & \text{if } \Phi.\text{reg}(r_2) = ((\_\_\_), \_\_\_, a) \quad \text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[getb} \, r_1 \, [\, r_2\, ]\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto \text{base}]) & \text{if } \Phi.\text{reg}(r_2) = ((\_\_\_), \_\_\_, \_\_\_) \quad \text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[gete} \, r_1 \, [\, r_2\, ]\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto \text{end}]) & \text{if } \Phi.\text{reg}(r_2) = ((\_\_\_), \_\_\_, \_\_\_\_, \_\_\_) \quad \text{and } \text{end} \neq \infty \\
\text{updatePc}(\Phi[\text{reg} \mapsto -42]) & \text{if } \Phi.\text{reg}(r_2) = ((\_\_\_), \_\_\_, \_\_\_\_, \_\_\_\_) \quad \text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[getp} \, r_1 \, [\, r_2\, ]\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto \text{encodePerm}(\text{perm})]) & \text{if } \Phi.\text{reg}(r_2) = ((\_\_\_, \_\_\_, \_\_\_\_, \_\_\_\_, \_\_\_\_, \_\_\_\_, \_\_\_\_) \quad \text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[getl} \, r_1 \, [\, r_2\, ]\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto \text{encodeLoc}(g)]) & \text{if } \Phi.\text{reg}(r_2) = ((\_\_\_, g), \_\_\_, \_\_\_) \quad \text{failed} & \text{otherwise} 
\end{cases} \]

\[\text{[isptr} \, r \, rv\, \text{]} \, (\Phi) = \begin{cases} 
\text{updatePc}(\Phi[\text{reg} \mapsto 1]) & \text{if } \Phi.\text{reg}(rv) \in \text{Cap} \quad \text{updatePc}(\Phi[\text{reg} \mapsto 0]) & \text{otherwise} 
\end{cases} \]
Define the following macros: restrict, subseg, and lea that does not overwrite the source register. A store that allows integers to be stored directly. store requires a register \( r_t \) for storage of temporary values to be available.

\[
\begin{align*}
\text{restrict } r_1 r_2 r_3 r_4 & \overset{\text{def}}{=} \text{move } r_1 r_2 \\
\text{restrict } r_1 r_3 r_4 & \\
\text{subseg } r_1 r_2 r_3 r_4 & \overset{\text{def}}{=} \text{move } r_1 r_2 \\
\text{subseg } r_1 r_3 r_4 & \\
\text{lea } r_1 r_2 r_3 & \overset{\text{def}}{=} \text{move } r_1 r_2 \\
\text{lea } r_1 r_3 & \\
\text{store } r n & \overset{\text{def}}{=} \text{move } r_t n \\
\text{store } r r_t &
\end{align*}
\]

**Lemma 1** (Determinacy). If \( \Phi \rightarrow \Phi' \) and \( \Phi \rightarrow \Phi'' \), then \( \Phi' = \Phi'' \). If \( \Phi \rightarrow_n \Phi' \) and \( \Phi \rightarrow_n \Phi'' \), then \( \Phi' = \Phi'' \). If \( \Phi \rightarrow_n \Phi' \) and \( \Phi \rightarrow_n' \) (halted, mem''), then \( n \leq n' \) and \( \Phi' \rightarrow_{n' - n} \) (halted, mem'').

\( \blacksquare \)

**Proof.** By easy inspection of the definition of the operational semantics. \( \Box \)
2 Malloc specification

**Specification 1** (Malloc Specification). $c_{\text{malloc}}$ *satisfies the specification for malloc iff*

$$c_{\text{malloc}} = ((E, \text{GLOBAL}), \omega, \perp) \land$$

$$\exists t_{\text{malloc},0}.$$ \[\forall i', \exists \iota_0. i', W(i) = \iota' \Rightarrow \iota'. H(i'.s)(\xi^{-1}((i \mapsto W(i)))) \land\]

$$t_{\text{malloc},0} \cdot v = \text{perm} \land$$

$$\forall \Phi \in \text{ExecConf}. \forall ms_{\text{footprint}}, ms_{\text{frame}} \in \text{MemSegment}.$$ \[\forall i, n, size \in \mathbb{N}. w_{\text{ret}} \in \text{Word}. \exists \Phi' \in \text{ExecConf}. \exists ms'_{\text{footprint}}, ms_{\text{alloc}} \in \text{MemSegment}. \exists j \in \mathbb{N}. j > 0 \land b', e' \in \text{Addr}. \exists t'_{\text{malloc}} \in \text{Region}. \] \[\Phi \to_j \Phi' \land\]

$$\Phi'. \text{mem} = ms'_{\text{footprint}} \cup ms_{\text{frame}}$$ \[\cup ms_{\text{footprint}} \cdot_{n-j} [i \mapsto t'_{\text{malloc}}] \land\]

$$t'_{\text{malloc}} \equiv_{\text{pub}} t_{\text{malloc}} \land$$

$$ms'_{\text{footprint}} \cdot_{n-j} [i \mapsto t'_{\text{malloc}}] \land$$

$$\text{dom}(ms_{\text{alloc}}) = \{b', e'\} \land \forall a \in [b', e']. ms_{\text{alloc}}(a) = 0 \land$$

$$\Phi'. \text{reg} = \Phi. \text{reg}((w_{\text{ret}}) \mapsto ((\text{Rwx}, \text{GLOBAL}), b', e', b')) \land$$

$$\Phi'. \text{reg}(r_1) = \text{size} \land \text{size} \geq 0 \land \Phi. \text{reg}(r_0) = w_{\text{ret}} \land$$

$$\Phi'. \text{reg}(pc) = \text{updatePcPerm}(c_{\text{malloc}}) \Rightarrow$$

$$\exists j \in \mathbb{N}. j > 0 \land \Phi' \to_j \text{failed}$$

In the specification above $t'_{\text{malloc}}$ is a future region of the initial region that governs malloc.

3 Macros

In order to write readable example programs, we provide macros (macro-instructions) that can be implemented in terms of the instruction set given in the formalisation.

In order to compute offsets and the like, the macros need registers to keep temporary computations in. We assume such a small set of registers $\text{RegisterName}_t \subseteq \text{RegisterName}$ is available and that $\text{RegisterName}_t$ does not contain registers explicitly named in a program nor $r_0, r_{\text{stk}}$, or pc (but clearing all registers still clears the temporary registers).

3.1 Linking and ABI

In order to make capabilities to trusted code (and possibly untrusted code) available, we assume that some sort of linker has made these available. This is done in the following way: For every function, the first memory cell the capability for that function governs contains a capability for
the linking table. Each function name in a program corresponds to an offset in the table, e.g., `malloc` could be at offset 0. When a name is used in a program, it indicates what entry from the linking table to pick. The table should always be accessible by taking a copy of the capability in the pc-register and adjusting it to point to the first cell it governs.

The capability linking table can be shared between multiple functions that are linked to the same capabilities as it is accessed through read-only capabilities.

### 3.2 Flag table

A function may use flags to signal failure. We use the convention that a flag table is available in the second memory cell of a functions code (so just after the linking table). The flag table is accessed through a read-write capability and initially it contains all zero. Like the linking table, each entry is associated with a name which may appear in the macros.

The flag table should never be shared between distrusting parties.

We will often want to make room in memory for a linking-table capability and a flag-table capability. We therefore define a constant that represents the offset of the actual code of a function caused by these two capabilities:

\[
\text{offsetLinkFlag} \overset{\text{def}}{=} 2
\]

### 3.3 Macro definitions

In the following, we describe each of the macros. The descriptions are so detailed that it should be a simple matter to implement the macros. We provide a proposed implementation for each of the macros in order to install some confidence in the fact that it is possible to implement each of the macro.

**fetch** \(r \ f\) load the entry of the linking table corresponding to \(f\) to register \(r\).
One possible malloc implementation (\(r\_t1\) and \(r\_t2\) are registers in RegName_t).

```
move r pc
getb r\_t1 r
geta r\_t2 r
minus r\_t1 r\_t1 r\_t2 // Offset to first address, i.e., linking table (b-a)
lea r r\_t1
load r r
lea r ... // ... replaced with offset to \(f\) in the linking table
move r\_t1 0
move r\_t2 0
load r r // \(f\) capability loaded to register r
```

**call** \(r(r_{args}, r_{prev})\)  
\(r_{args}\) and \(r_{prev}\) are lists of registers. An overview of this call:
- Set up activation record
- Create local enter capability for activation (protected return pointer)
- Clear unused registers
- Jump
- Upon return: Run activation code

---

10
A more detailed description of each of the above steps:

**Set up activation record**

- Run malloc to get a piece of memory with space for:
  - Words in $r_{priv}$
  - Code return capability (opc)
  - Activation code
- Store the words in $r_{priv}$ to the activation record.
- Adjust a copy of the current pc to point to the return address in code and save it to the activation record.
- Write the activation code to the activation record.

**Create local enter capability for activation** Adjust the capability for the activation record to point to the beginning of the activation record and restrict it to a local enter-capability. Place this capability in $r_0$.

**Clear unused registers** Clear all the register that are not pc, r, $r_0$ or in $r_{args}$.

**Jump** Jump to register $r$

**Activation code** The activation code does the following:

- Move the stored “private” words in to their respective $r_{priv}$ registers.
- Load the return capability to pc

Possible implementation. We will use `malloc r n` and `rclear` (defined below). Assume $r_{priv} = r_{priv,1}, \ldots, r_{priv,n}$

```plaintext
malloc r_t ... // ... is the size of activation record
// store private state in activation record
store r_t r_priv,1
lea r_t 1
store r_t r_priv,2
lea r_t 1
...
lea r_t 1
store r_t r_priv,n
lea r_t 1
// store old pc
move r_t1 pc
lea r_t1 ... // ... is the offset to return address
store r_t r_t1
lea r_t1 1
// store activation record
store r_t encode(i_1)
lea r_t1 1
...
lea r_t1 1
store r_t encode(i_m)
lea r_t1 k // k is m-1, i.e. the offset to the first instruction of the activation code.
restrict r_t1 encodePermPair((Local,e))
move r_0 r_t1
```
rclear R // R = RegisterName - {r,pc,r_0,r_args}
jmp r

Activation record. The instructions correspond to $i_1, \ldots, i_m$ in the above.

\begin{verbatim}
move r_t pc
getb r_t1 r_t
geta r_t2 r_t
minus r_t1 r_t1 r_t2
// load private state
lea r_t r_t1
load r_priv,1 r_t
lea r_t 1
load r_priv,2 r_t
lea r_t 1
...  
lea r_t 1
load r_priv,n r_t
lea r_t 1
// load old pc
load pc r_t
\end{verbatim}

malloc $r$ $n$ Calls malloc to allocates a piece of memory of size $n$. The capability will be stored in register $r$. One possible malloc implementation ($r_t1$ is a register in RegName_t) and $r_1$ is the register from the malloc specification.

\begin{verbatim}
fetch r malloc
move r_1 n
// save return pointer
move r_t1 r_0
// setup new return pointer
move r_0 pc
lea r_0 4 // 4 is the offset to just after jmp r
restrict r_0 encodePerm(e)
jmp r
move r r_1
move r_0 r_t1 // restore return pointer
move r_1 0
move r_t1 0
\end{verbatim}

assert$\text{flag}$ $r_1$ $r_2$ Compares the words in register $r_1$ and $r_2$ (if one of them is an integer, then use that in the comparison). If they are equal, then execution continues. If they are unequal, then the assertion flag named $\text{flag}$ in the flag list is set to 1 and execution halts (if no flag is specified, then the first flag in the list is set to 1).

There are four different asserts based on whether $r_1$ and $r_2$ are registers or numbers. If $r_1$ and $r_2$ are registers:

\begin{verbatim}
// setup pointer to fail.
move r_t3 pc
lea r_t3 ... // ... is the offset to fail
// make sure both registers contain either capability or integer
\end{verbatim}
isptr r_t1 r_1
isptr r_t2 r_2
minus r_t1 r_t1 r_t2
jnz r_t3 r_t1

// set up capability for cap case:
move r_t4 pc
lea r_t4 ... // ... is the offset to caps
jnz r_t4 r_t2 // jump to caps if r_t2 contains a capability

// the two registers contain an integer
minus r_t1 r_1 r_2
jnz r_t3 r_t1

// the two integers in the registers are equal
move r_t4 pc
lea r_t4 ... // .. offset to success

caps:

geta r_t1 r_1
geta r_t2 r_2
minus r_t1 r_t1 r_t2
jnz r_t3 r_t1
getb r_t1 r_1
getb r_t2 r_2
minus r_t1 r_t1 r_t2
jnz r_t3 r_t1
gete r_t1 r_1
gete r_t2 r_2
minus r_t1 r_t1 r_t2
jnz r_t3 r_t1
getp r_t1 r_1
getp r_t2 r_2
minus r_t1 r_t1 r_t2
jnz r_t3 r_t1
getl r_t1 r_1
getl r_t2 r_2
minus r_t1 r_t1 r_t2
jnz r_t3 r_t1

// the two capabilities in the registers are equal
move r_t4 pc
lea r_t4 ... // .. offset to success

fail:

// get the flag capability
move r_t3 pc
getb r_t1 pc
geta r_t2 pc
minus r_t1 r_t1 r_t2
lea r_t3 r_t1
lea r_t3 1 // the flag table capability is at the second address of cap.
load r_t1 r_t3
lea r_t1 ... // ... is the offset of flag in the table
store r_t1 1
halt

success:
   // clean up
   move r_t1 0
   move r_t2 0
   move r_t3 0
   move r_t4 0

If \( r_1 \) is a register, but \( r_2 \) is a constant:
   // setup pointer to fail.
   move r_t3 pc
   lea r_t3 ... // ... is the offset to fail
   // make sure both registers contain either capability or integer
   isptr r_t1 r_1
   jnz r_t3 r_t1
   minus r_t1 r_1 r_2
   jnz r_t3 r_t1
   // the two integers in the registers are equal
   move r_t3 pc
   lea r_t3 ... // ... offset to success

fail:
   // get the flag capability
   move r_t3 pc
   getb r_t1 pc
   geta r_t2 pc
   minus r_t2 r_t1 r_t2
   lea r_t3 r_t1
   lea r_t3 1 // the flag table capability is at the second address of cap.
   load r_t1 r_t3
   lea r_t1 ... // ... is the offset of flag in the table
   store r_t1 1
   halt

success:
   // clean up
   move r_t1 0
   move r_t3 0

The case where \( r_1 \) is a constant and \( r_2 \) is a register is omitted. The case where both are
constant is also omitted - if the constants are the same, then the macro is nothing. If they
are different, then it corresponds to the failed part of both of the above implementations.

\textit{mclear} \( r \) Stores 0 to all the memory cells the capability \( r \) governs\(^1\).

Possible implementation:
   move r_t r
   getb r_t1 r_t
   geta r_t2 r_t
   minus r_t2 r_t1 r_t2

\(^1\)This may in some cases seem like an unreasonable slow instruction. In a real system it would probably be
implemented as a vector operation which allows modification of continuous segments of memory rather fast.
lea r_t r_t2
gete r_t2
minus r_t1 r_t2 r_t1
plus r_t1 r_t1 1
move r_t2 pc
lea r_t2 ... // ... is the offset to end
move r_t3 pc
lea r_t3 ... // ... is the offset to iter

iter:
  jnz r_t2 r_t1
  store r_t 0
  lea r_t 1
  plus r_t1 r_t1 1
  jmp r_t3

end:
  move r_t 0
  move r_t1 0
  move r_t2 0
  move r_t3 0

rclear \bar r \ Move 0 to all the registers in the list \bar r.
Possible implementation: Say \bar r = r_1,\ldots,r_n

move r_1 0
move r_2 0
// ...
move r_n 0

Note:

- call will fail if we have local capabilities in one of the registers of the “private” register list
  as it relies on a capability returned by malloc which will not be permit-write-local. This
  severely limits how scall can be used and it provides very little in terms of control-flow
  integrity when nested. Below, we introduce scall which can handle local capabilities in
  the “private” state.

3.4 Stack

Some programs will assume access to a stack which will be in part indicated by the program
macros but also in the correctness lemma. The stack is accessed through a local rwlx-capability.
Programs will assume that the stack resides in some register, say r_stk.

The stack resides entirely in memory. There is no separation between the memory and the
stack, so when we talk about the stack it is as a conceptual thing.

Even though the memory is infinite, we will only use a finite part for the stack. If we
have allocated too little memory for the stack, and we try to push something anyway, then the
execution will fail. As we consider failing admissible, we are okay with this.

When not in the middle of a push or a pop, the stack capability points to the top word of
the stack. For an empty stack, the stack capability points to the address just below of the range
of authority for the stack capability.

The stack grows upwards
**push** \( r \) Pushes the word in register \( r \) to the stack by incrementing the address of the stack capability by one and storing the word through the stack capability.

Possible implementation:

\[
\begin{align*}
\text{lea} & \quad r_{\text{stk}} \quad 1 \\
\text{store} & \quad r_{\text{stk}} \quad r
\end{align*}
\]

**pop** \( r \) Pops the top word of the stack by loading it to register \( r \), and decrementing the address of the stack capability.

\[
\begin{align*}
\text{load} & \quad r \quad r_{\text{stk}} \\
\text{minus} & \quad r_{t1} \quad 0 \quad 1 \\
\text{lea} & \quad r_{\text{stk}} \quad r_{t1}
\end{align*}
\]

**SCALL** \( r(r_{args}, r_{prev}) \)

\( r_{args} \) and \( r_{prev} \) are lists of registers. This call assumes \( r_{stk} \) contains a stack capability. An overview of this call:

- Push “private” registers to the stack.
- Push the restore code to the stack.
- Push return address capability
- Push stack capability
- Create protected return pointer
- Restrict stack capability to unused part
- Clear the part of the stack we release control over
- Clear unused registers
- Jump
- Upon return: Run the on stack restore code
- Return address in caller-code: Restore “private” state

A more detailed description of the above steps:

**Push “private” registers to the stack** Push all the words in the registers in \( r_{prev} \) to the stack.

**Push the restore code to the stack** Push the restore code to the stack (described later). This code needs to be on the stack to make sure the stack capability can be restored. We keep the restore code on the stack minimal. The caller code does the rest of the restoration.

**Push return address capability** Push a capability for the return address (in the memory) to the stack.

**Push stack capability** Push the full stack capability to the stack.

**Create protected return pointer** Make a new version of the stack pointer that points to the beginning of the restoration code. Restrict it to a local enter-capability and put it in \( r_0 \).

**Restrict stack capability to unused part** Make the stack capability only govern the unused part.
Clear the part of the stack we release control over  Store 0 to all the memory cells the restricted stack pointer has authority over.

Clear unused registers  Clear all registers but pc, r, r0, rstk, and rargs.

Jump  Jump to register r.

Run the on stack restore code  Load the stack capability to rstk. Pop the old program counter (the return address in caller-code) from the stack to pc.

Return address in caller-code: Restore “private” state

- Pop the restore code of the stack
- Pop the private state on the stack into their respective rpriv registers.

Possible implementation, say rargs = rargs1,...,rargsn and rpriv = rpriv1,...,rprinn:

```
// push private state
push r_priv,1  
...  
push r_priv,n
// push activation code
push encode(i_1)
...  
push encode(i_4)
// push old pc
move r_t1 pc  
lea r_t1 ... // ... is the offset to after
push r_t1
// push stack pointer
push r_stk
// set up protected return pointer
move r_0 r_stk  
lea r_0 -5 // -5 is the offset to the first instruction of the activation code
restrict r_0 encodePermPair((Local,e))
// restrict stack capability
geta r_t1 r_stk  
plus r_t1 r_t1 1
getb r_t2 r_stk
subseg r_stk r_t1 r_t2
// clear unused part of the stack
mclear r_stk
// clear non-argument registers
rclear R // where R = RegisterName - {pc,r_stk,r_0,r,r_args}
jmp r
after:
// pop the restore code
pop r_t1  
pop r_t1
pop r_t1
pop r_t1
pop r_t1
```
// pop the private state into appropriate registers
pop r_priv,1
...
pop r_priv,n
where the restore code is as follows:

\[ \begin{align*}
    i_1 &= \text{move } r_{t1} \text{ pc} \\
    i_2 &= \text{lea } r_{t1} 5 \quad \text{// 5 is the offset to the address where the old stack pointer is located} \\
    i_3 &= \text{load } r_{stk} \ r_{t1} \\
    i_4 &= \text{pop } \text{pc}
\end{align*} \]

Note:

- If we want to have local capabilities as part of our private state, then we need to have a stack and use `scall`. If we do not have any local capabilities we want to keep around, then we can use `call`, but it will incur a small memory leak as the activation records cannot be recycled! It is also possible to use a combination of `scall` and `call`, but when `call` is used, then we have no way to store the stack, so we cannot use `scall` after that.

- As a rule of thumb: If you have provided an untrusted entity access to part of the stack, then it needs to be cleared before it is passed to an untrusted party.

- As a rule of thumb: If you receive a stack from an untrusted source, then you need to check that it is a local `rwlx`-capability and clear it! If any callbacks are provided, then they need to be global.

\[ \text{crtcls \{ (x_1,r_1),..., (x_n,r_n) \} } \]

\[ \text{rcode} \]

\[ \{ (x_1,r_1),..., (x_n,r_n) \} \] is a list of variable bindings. If an instruction refers to a variable, then it will assume that an environment is available in a designated register (say \( r_{\text{env}} \)). The register \( r_{\text{code}} \) should contain a capability governs the code of the closure and that is executable when jumped to.

Allocate memory for variable environment

Store register contents to environment

Allocate memory for record with environment capability, code capability, and activation code

Store capabilities and activation code to record

Restrict the capability for the “closure pair” to an enter capability

Activation code:

- Load the environment capability to a designated register
- Load the code capability.
- Jump to the code.

A more detailed description of each step:

Allocate memory for variable environment Have malloc allocate a piece of memory of size \( n \) (the size of the variable environment).

Store register contents to environment Store the contents of each of the registers \( r_1,\ldots,r_n \) to the newly allocated memory.
Allocate memory for record with environment capability, code capability, and activation code

Allocate a new piece of memory with room for a capability for the environment.

**Store capabilities and activation code to record** Store the environment capability and code capability in the record followed by the activation code.

**Restrict the capability for the “closure pair” to an enter capability** Adjust the capability to point to the start of the activation code and restrict it to a global enter-capability.

**Activation code:**

- Load the environment capability to a designated register.
- Load the code capability.
- Jump to the code.

Possible implementation of \(\text{crtcls} (x, r_v) r_{\text{code}}\) where \(|(x, r_v)| = n\) (i.e. the activation code, is defined later):

```plaintext
malloc r_t1 n
store r_t1 r_v1
lea r_t1 1
store r_t1 r_v2
lea r_t1 1
... 
lea r_t1 1
store r_t1 r_vn
lea r_t1 -n
restrict r_t1 encodePermPair((Global,rw))
malloc r_1 8 //length of activation record
store r_1 r_code // code capability
lea r_1 1
store r_1 r_t1 // environment capability
move r_t1 0
lea r_1 1
store r_1 encode(i_1)
lea r_1 1
store r_1 encode(i_2)
lea r_1 1
... 
lea r_1 1
store r_1 encode(i_6)
lea r_1 -5 //offset to first instruction
restrict r_1 encodePerm(e)
```

Activation code \((i_1,...,i_6)\):

```plaintext
i_1 = move r_t1 pc
i_2 = lea r_t1 -2
i_3 = load r_env r_t1
i_4 = lea r_t1 1
i_5 = load r_t1 r_t1
i_6 = jmp r_t1
```
load $r$ $x$ Assumes environment capability available in register $r_{env}$. Loads the word at the index associated with $x$ in the environment list. Loads from this capability into $r$.
Possible implementation:

```
move r_t1 r_env
lea r_t1 ... // ... corresponds to offset of $x$ in environment
load r r_t1
move r_t1 0
```

store $x$ $r$ Assumes environment capability available in register $r_{env}$. Loads the word at the index associated with $x$ in the environment list. Stores the contents of register $r$ through this capability.

```
move r_t1 r_env
lea r_t1 ... // ... corresponds to offset of $x$ in environment
store r_t1 r
move r_t1 0
```

regglob $r$ Tests if register $r$ contains a GLOBAL capability. If not fail, otherwise continue execution.
Possible implementation:

```
getl r_t1 r
minus r_t1 r_t1 encodeLoc(Global)
move r_t2 pc
lea r_t2 4 // 4 is the offset to just after fail
jnz r_t1 r_t2
fail
move r_t1 0
move r_t2 0
```

reperm $r$ $n$ Tests if register $r$ contains a capability with permission $decodePerm(n)$. If not fail, otherwise continue execution.
Possible implementation:

```
getp r_t1 r
minus r_t1 r_t1 n
move r_t2 pc
lea r_t2 4 // 4 is the offset to just after fail
jnz r_t1 r_t2
fail
move r_t1 0
move r_t2 0
```

prepstack $r$ Tests if register $r$ contains a capability with permission RWLX. If not fail, otherwise assume $r$ points to $((RWLX, g), base, end, a)$ adjust it to $((RWLX, g), base, end, base - 1)$.
Possible implementation

```
reperm r encodePerm(rwlx)
getb r_t1 r
geta r_t2 r
```
Figure 3: This is the first figure of 6 that illustrates how \texttt{scall} works. In this example, the call \texttt{scall r([r_arg1, \ldots, r_arg_n], [r_0, r_{priv1}, \ldots, r_{priv_m}])}. In this example the two lists of registers are disjoint even though that does not have to be the case.

\begin{verbatim}
minus r_t1 r_t1 r_t2
lea r r_t1
minus r_t1 0 1
lea r r_t1
move r_t1 0
move r_t2 0
\end{verbatim}

**Note:**

- In a real setting due to a limited number of registers, some of the arguments might be spilled to the stack. It would be possible to do something similar here, but to keep matters simple, we opt not to do so.

- \texttt{reqperm} can be used to test whether something can pass as a stack.

- \texttt{reqglob} can be used to test whether a callback is admissible in the presence of a stack.

- The code of a closure will often be found in conjunction with the code that creates it.

- \texttt{prepstack} as “prepare stack”. This ensures that the register contains something that looks like a stack and it is prepared for our stack convention.

### 3.5 Labels

1: is a meta level label that can be used to refer to a specific address. When placed on the line of a macro, it refers to the first instruction of this macro.
Figure 4: Stack and register-file after the restore code, “private” registers (remember \(r_0\) is here private.), return address (\(c'_{pc}\)), and stack capability (\(c'_{stk}\)) have been pushed to the stack.

Figure 5: Stack and register-file after the \(c'_{stk}\) has been limited to only give authority over the empty part of the stack (the new capability is \(c''_{stk}\)). The empty part of the stack has been cleared. \(c'_{0}\) is made from \(c'_{stk}\) by setting it to point to the restore code and restricting it to a local enter-capability. The “private” registers have been cleared.
Figure 6: Stack and register-file upon return from \( f \). At this point we have no idea what is in the register-file apart from the pc which we know points to the restore code. The contents of the stack we released access to is also unknown. (Notice that we have changed the order of the registers as we are no longer interested in the argument registers. By convention we expect a return value to be in \( r_1 \), which is why we have named that word, but the words in the remaining non-special-purpose registers could also be considered return values.)

Figure 7: Stack and register-file after executing the restore code. The old stack capability has been restored and the pc-register now points to the return address in memory.
Figure 8: Stack and register-register file after the clean up code has been run. The “private” words have been popped to their respective registers. The restore code has been popped off the stack.
4 Examples

4.1 Encapsulation of Local State

Assembly program not using stack. Assume that \( r_l \not\in \{pc, r_0\} \) is a register.

\[
f1: \text{malloc } r_l 1
\]
\[
\text{store } r_l 1
\]
\[
\text{fetch } r_{\text{adv}} \text{ adv}
\]
\[
\text{call } r_{\text{adv}}([], [r_l])
\]
\[
\text{assert } r_l 1
\]
\[
\text{if: halt}
\]

For \( f1 \) to work, its local state needs to be encapsulated.

**Lemma 2** (Correctness lemma for \( f1 \)).

For all \( n \in \mathbb{N} \) let

\[
c_{\text{adv}} \triangleq (\text{E, GLOBAL}, \text{base}_{\text{adv}}, \text{end}_{\text{adv}}, \text{base}_{\text{adv}} + \text{offsetLinkFlag})
\]
\[
c_{f1} \triangleq ((\text{RW}, \text{GLOBAL}), f1 - \text{offsetLinkFlag}, \text{if}, f1)
\]
\[
c_{\text{malloc}} \triangleq ((\text{E, GLOBAL}), \text{base}_{\text{malloc}}, \text{end}_{\text{malloc}}, \text{base}_{\text{malloc}} + \text{offsetLinkFlag})
\]
\[
m \triangleq ms_{f1} \sqcup ms_{\text{flag}} \sqcup ms_{\text{link}} \sqcup ms_{\text{adv}} \sqcup ms_{\text{malloc}} \sqcup ms_{\text{frame}}
\]

and

- \( ms_{\text{malloc}} \) satisfies the specification for \( \text{malloc} \) and \( t_{\text{malloc}, 0} \) is the region from the specification.

where

\[
\text{dom}(ms_{f1}) = [f1 - \text{offsetLinkFlag}, \text{if}]
\]
\[
\text{dom}(ms_{\text{flag}}) = [\text{flag}, \text{flag}]
\]
\[
\text{dom}(ms_{\text{link}}) = [\text{link}, \text{link} + 1]
\]
\[
\text{dom}(ms_{\text{adv}}) = [\text{base}_{\text{adv}}, \text{end}_{\text{adv}}]
\]
\[
ms_{\text{malloc}} \cdot [0 \mapsto t_{\text{malloc}, 0}]
\]

and

- \( ms_{f1}(f1 - \text{offsetLinkFlag}) = ((\text{RO}, \text{GLOBAL}), \text{link}, \text{link} + 1, \text{link}), ms_{f1}(f1 - \text{offsetLinkFlag} + 1) = ((\text{RW}, \text{GLOBAL}), \text{flag}, \text{flag}, \text{flag}), \) the rest of \( ms_{f1} \) contains the code of \( f1 \).

- \( ms_{\text{flag}} = [\text{flag} \mapsto 0] \)

- \( ms_{\text{link}} = [\text{link} \mapsto c_{\text{malloc}}, \text{link} + 1 \mapsto c_{\text{adv}}] \)

- \( ms_{\text{adv}} \) contains a global read-only capability for \( ms_{\text{link}} \) on its first address. The remaining cells of the memory segment only contain instructions.

If

\[
(reg[pc \mapsto c_{f1}], m) \rightarrow_n (\text{halted}, m')
\]

then

\[
m'(\text{flag}) = 0
\]
Proof of Lemma 2. Let \( n \) be given and assume the premises in the lemma. Consider the following part of the execution:

\[
(reg[pc \mapsto c_{f1}], m) \rightarrow (reg_0[pc \mapsto c_{malloc}][r_0 \mapsto c'_{f1}][r_1 \mapsto 1], m)
\]

Where \( c'_{f1} \) is the return address. Use the malloc specification with

\[
\begin{align*}
\iota_{malloc} &= \iota_{malloc,0} \\
\text{ms}_{footprint} &= \text{ms}_{malloc} \\
\Phi, \text{reg}(r_1) &= \text{size} = 1
\end{align*}
\]

to get

\[
(reg_0[pc \mapsto c_{malloc}][r_0 \mapsto c'_{f1}][r_1 \mapsto 1], m) \rightarrow (reg_0[pc \mapsto c_{malloc}][r_0 \mapsto c'_{f1}][r_1 \mapsto c_l], m')
\]

for some \( j \) where for some \( \iota'_{malloc} \equiv \text{pub} \iota_{malloc,0} \)

1. \( m' = \text{ms}_{f1} \oplus \text{ms}_{flag} \oplus \text{ms}_{link} \oplus \text{ms}_{adv} \oplus \text{ms}_{ar} \oplus \text{ms}_{malloc} \oplus \text{ms}_{frame} \)
2. \( \text{ms}'_{malloc} \cdot n - j \ [0 \mapsto \iota_{malloc}] \)
3. \( \text{dom}(\text{ms}_{l}) = [l, l] \)
4. \( c_l = ((\text{rwx, global}), l, l, l) \)
5. \( \text{ms}_{l}(l) = 0 \)

Continue the execution to the next malloc hidden in \texttt{call}.

\[
(reg_0[pc \mapsto c'_{f1}][r_0 \mapsto c'_{f1}][r_1 \mapsto c_l], m') \rightarrow (reg_0[pc \mapsto c_{malloc}][r_0 \mapsto c'_{f1}][r_1 \mapsto \text{len}_{ar}][r_1 \mapsto c_l], m'')
\]

where

6. \( m'' = m'\ [l \mapsto 1] \)

Use the malloc specification notice:

- \( \text{len}_{ar} \) is the needed size for the activation record.
- \( \text{ms}_{footprint} = \text{ms}'_{malloc} \)

Get:

\[
(reg_0[pc \mapsto c_{malloc}][r_0 \mapsto c''_{f1}][r_1 \mapsto \text{len}_{ar}][r_1 \mapsto c_l], m'') \rightarrow (reg_0[pc \mapsto c''_{f1}][r_0 \mapsto c''_{f1}][r_1 \mapsto c_{ar}][r_1 \mapsto c_l], m''(3))
\]

for some \( j' \) where for some \( [0 \mapsto \iota'_{malloc}] \equiv \text{pub} [0 \mapsto \iota_{malloc}] \)

7. \( m'' = \text{ms}_{f1} \oplus \text{ms}_{flag} \oplus \text{ms}_{link} \oplus \text{ms}_{adv} \oplus \text{ms}_{ar} \oplus \text{ms}_{malloc} \oplus \text{ms}_{frame} \)
8. \( \text{ms}'_{malloc} \cdot n - j' \ [0 \mapsto \iota'_{malloc}] \)
9. \( \text{dom}(\text{ms}_{ar}) = [b, e] \), and \( e - b = \text{len}_{ar} \)
10. \( c_l = ((\text{rwx, global}), b, e, b) \)
11. \( \forall a \in [b, c]. ms_ar(a) = 0 \)

Continue execution until just after the jump to \( adv \).

\[
(reg_0[pc \mapsto c_f'[1]][r_0 \mapsto c'_f][r_1 \mapsto c_{ar}][r_1 \mapsto c_i], m^{(3)}) \rightarrow_{k'} (reg_0[pc \mapsto:updatePcPerm(c_{adv})][r_1 \mapsto c_{adv}][r_0 \mapsto c'_ar], m^{(3)})
\]

for some \( k' \) where

- \( m^{(3)} = ms_f \sqcup msflag \sqcup mslink \sqcup ms_{adv} \sqcup ms_l \sqcup ms_{ar}' \sqcup ms_{malloc}' \sqcup ms_{frame} \)

- \( ms_{ar}' \) contains the activation record, i.e., \( c_{ar}, c'_{f1} \) (the return address in \( f1 \)), and activation code.

- \( c_{ar}' = ((E, LOCAL)b, c, b + offset) \) where \( b + offset \) is the first address of the activation code.

Define

\[
W = [0 \mapsto \ell'_{malloc}][1 \mapsto \ell'_{base_{adv}, end_{adv}}][2 \mapsto \ell s\{perm, ms_f \sqcup ms_{ar} \sqcup ms_l \sqcup ms_{flag}\}][3 \mapsto \ell_{malloc}]
\]

define

1. \( ms = ms_f \sqcup msflag \sqcup mslink \sqcup ms_{adv} \sqcup ms_l \sqcup ms_{ar}' \sqcup ms_{malloc}' \)

Use the FTLR on \( updatePcPerm(c_{adv}) \) using world \( W \), so show

- \( (n, (base_{adv}, end_{adv})) \in readCondition(GLOBAL)(W) \)
  - Show: \( \ell_{base_{adv}, end_{adv}} \overset{n}{\subseteq} \ell_{base_{adv}, end_{adv}} \): Follows from Lemma 22.

Have

2. \( (n, updatePcPerm(c_{adv})) \in \mathcal{E}(W) \)

Let \( n' = n - j - j' - k - k' \) and show

1. \( ms_{n'}, W \)

1.1. Split the memory into the disjoint unions of 1 and show:

1.1.1. case: \( (n', ms_{malloc}) \in \ell_{malloc}.H(\ell_{malloc}.s)(W) \)
  - Use \( ms_{malloc} \cdot n'[0 \mapsto \ell_{malloc}] \) with malloc specification context independence property.

1.1.2. case: \( (n', ms_{adv}) \in H^{\ell_{malloc}}_{base_{adv}, end_{adv}}1W \)
  - Show \( \forall a \in [base_{adv}, end_{adv}].((n' - 1, ms(a)) \in \mathcal{V}(W) \land ms(a) \text{ is non-local}) \)
  - \( a \neq base_{adv} : \) trivial, contains instruction only and they are non-local.
  - \( a = base_{adv} : \) show \( ((\text{RO, GLOBAL}, link, link + 1, link) \in \mathcal{V}(W) \land \text{GLOBAL capabilities are non-local}) \)

\[ \text{SFTS } \ell_{base_{adv},end_{adv}}(perm, ms_{link}) \overset{n'_{i}}{\subseteq} \ell_{link,link+1} \text{ which follows from Lemma 23.} \]

1.1.3. \( (n', ms_{link}) \in H^{\ell_{malloc}}_{base_{adv}, end_{adv}}(W) \):
  - This boils down to showing:
    1.1.3.1. \( (n' - 1, \ell_{malloc}) \in \mathcal{V}(W) \): Follows from Lemma 50.
1.1.3.2. \((n'-1,c_{adv}) \in V(W)\): for \(n'' < n'-1\) and \(W' \sqsubseteq^\text{priv} W\) show:
\((n'', \text{updatePcPerm}(c_{adv})) \in E(W')\). Follows from Lemma 49, together with Lemma 79 and the fact that \(c_{adv}\) is non-local.

1.1.4. The last case follows from Lemma 67.

2. \((n', c_{adv}) \in V(W)\)

2.1. case: \((n', c_{adv}) \in V(W)\)

2.1.1. Similar to 1.1.3.2.

2.2. case: \((n', c'_{ar}) \in V(W)\)

2.2.1. Let \(n'' < n'\) and \(W' \sqsubseteq^\text{pub} W\) be given and show \((n'', \text{updatePcPerm}(c'_{ar})) \in E(W')\)
Let \(n^{(3)} \leq n''\), \(ms' : n^{(3)} W'\), and \((n^{(3)}, \text{reg})\) be given
Show: \((n^{(3)}, (\text{reg}[pc \mapsto \text{updatePcPerm}(c'_{ar})], ms')) \in O(W')\)
Assume \((\text{reg}[pc \mapsto \text{updatePcPerm}(c'_{ar})], ms' \uplus ms_{frame}) \rightarrow_{k''} (\text{halted}, m')\), for some \(k'' \leq n^{(3)}\), \(m'\) and \(ms_{frame}\). Due to \(ms' : n^{(3)} W'\), \(ms_{f1}, ms_{flag}, ms'_{ar},\) and \(ms_{l}\) are unchanged.
The execution loads \(c_{l}\) to \(r_{l}\) and jumps to \(f^{(3)}\) (the point just before the assertion). As \(ms_{l} = 1\), the assertion is successful and the execution halts. In other words, there were no changes to the memory.
Use \(W'\), \(ms_{r} = \emptyset\), and \(ms'\) to get the desired result, i.e., \(m' = ms' \uplus ms_{frame}\) and \(ms' : n^{(3)}-k'' W'\) (using downwards closure of memory satisfaction).

2.3. case: \((n', 0) \in V(W)\) (the contents remaining registers)
Trivial to show.

Get
\((n', (\text{reg}[pc \mapsto \text{updatePcPerm}(c_{adv})][r_1 \mapsto c_{adv}][r_0 \mapsto c'_{ar}], m^{(3)}) \in O(W)\)

By initial assumption of the lemma, the execution halts. Use \(ms_{frame}, m'\) and the number of steps it takes to halt to get: \(W' \sqsubseteq^\text{priv} W, ms_{r}\) and \(ms'\) s.t. \(m' = ms_{r} \uplus ms' \uplus ms_{frame}\) and \(ms' : n W'\). As \(\iota_{flag}\) is a permanent region, we know it is still in \(W'\), so \(m'(\text{flag}) = 0\).

4.2 Encapsulation of Local State Using Local Capabilities and scall

Assembly program using the stack. This program assumes a \(r_{stk} \notin \{pc, r_{0}\}\) register that contains a stack capability (a local RWLX-capability):

```
f2: push 1
    fetch r1 adv
    scall r1([], [])
pop r1
assert r1 1
2f: halt
```
Lemma 3 (Correctness lemma for \( f_2 \)).

Let

\[
\begin{align*}
c_{adv} & \overset{\text{def}}{=} ((\text{E, GLOBAL}), \text{base}_{adv}, \text{end}_{adv}, \text{base}_{adv} + \text{offsetLinkFlag}) \\
c_{f_2} & \overset{\text{def}}{=} ((\text{RWX, GLOBAL}), f_2 - \text{offsetLinkFlag}, 2f, f_2) \\
c_{malloc} & \overset{\text{def}}{=} ((\text{E, GLOBAL}), \text{base}_{malloc}, \text{end}_{malloc}, \text{base}_{malloc} + \text{offsetLinkFlag}) \\
c_{stk} & \overset{\text{def}}{=} ((\text{RWLX, LOCAL}), \text{base}_{stk}, \text{end}_{stk}, \text{base}_{stk} - 1) \\
c_{link} & \overset{\text{def}}{=} ((\text{RO, GLOBAL}), \text{link}, \text{link} + 1, \text{link}) \\
\end{align*}
\]

\( \text{reg} \in \text{Reg} \)

\[
m \overset{\text{def}}{=} ms_{f_2} \uplus ms_{flag} \uplus ms_{link} \uplus ms_{adv} \uplus ms_{malloc} \uplus ms_{stk} \uplus ms_{frame}
\]

and

- \( c_{malloc} \) satisfies the specification for malloc and \( \iota_{malloc,0} \) is the region from the specification.

where

\[
\begin{align*}
\text{dom}(ms_{f_2}) &= [f_2 - \text{offsetLinkFlag}, 2f] \\
\text{dom}(ms_{flag}) &= [\text{flag}, \text{flag}] \\
\text{dom}(ms_{link}) &= [\text{link}, \text{link} + 1] \\
\text{dom}(ms_{stk}) &= [\text{base}_{stk}, \text{end}_{stk}] \\
\text{dom}(ms_{adv}) &= [\text{base}_{adv}, \text{end}_{adv}] \\
ms_{malloc} : n \mapsto \iota_{malloc,0} & \quad \text{for all } n \in \mathbb{N}
\end{align*}
\]

and

- \( ms_{f_2}(f_2 - \text{offsetLinkFlag}) = ((\text{RO, GLOBAL}), \text{link}, \text{link} + 1, \text{link}), ms_{f_2}(f_2 - \text{offsetLinkFlag} + 1) = ((\text{RW}, \text{GLOBAL}), \text{flag}, \text{flag}, \text{flag}), \) the rest of \( ms_{f_2} \) contains the code of \( f_2 \).

- \( ms_{flag} = [\text{flag} \mapsto 0] \)

- \( ms_{link} = [\text{link} \mapsto c_{malloc}, \text{link} + 1 \mapsto c_{adv}] \)

- \( ms_{adv}(\text{base}_{adv}) = c_{link} \) and \( \forall a \in [\text{base}_{adv} + 1, \text{end}], ms_{adv}(a) \in \mathbb{Z} \)

if

\[
(\text{reg}[pc \mapsto c_{f_2}[r_{stk} \mapsto c_{stk}], m]) \rightarrow_n (\text{halted}, m'),
\]

then

\[
m'(\text{flag}) = 0
\]

Proof of Lemma 3 (using scall lemma). Let \( n \) be given and make the assumptions of the lemma. If we can show

\[
(\text{reg}[pc \mapsto c_{f_2}[r_{stk} \mapsto c_{stk}], m \uplus ms_{stk}) \in O(W) \quad \text{for}
\]

\[
ms = ms_{f_2} \uplus ms_{flag} \uplus ms_{link} \uplus ms_{adv} \uplus ms_{malloc}
\]

and

\[
W = [0 \mapsto \iota_{malloc,0}] | 1 \mapsto \tau^{sta}(\text{perm}, ms_{f_2} \uplus ms_{flag})| 2 \mapsto \tau^{sta, u}(\text{perm, ms_{link}})| 3 \mapsto \tau^{nwl,p}_{base_{adv}, end_{adv}}
\]
then we are done as we by assumption has

\[(\text{reg}[\text{pc} \mapsto c_f2][\text{r}_{\text{stk}} \mapsto c_{\text{stk}}], m) \rightarrow_n (\text{halted}, m')\]

so \(1\) gives us a \(\hat{W}' \ni_{\text{priv}} W\) where \(W'\) satisfy part of \(m'\). As \(ms_{\text{flag}}\) is governed by a perm region, so it is unchanged. In other words

\[m'(\text{flag}) = 0\]

So it suffices to show \(1\). To this end use Lemma \(8\) Let \(ms_f\) be given, then

\[(\text{reg}[\text{pc} \mapsto c_f2][\text{r}_{\text{stk}} \mapsto c_{\text{stk}}], ms \uplus ms_{\text{stk}} \uplus ms_f) \rightarrow_k (\text{reg}', ms \uplus ms'_{\text{stk}} \uplus ms_f)\]

where

- \((\text{reg}', ms)\) is looking at \(\text{call} r_{\text{adv}}([][\text{r}_1])\) followed by \(c_{\text{next}}\)
- \(c_{\text{next}}\) is \(c_f2\) that points to the instruction after the \(\text{call}\).
- \(\text{reg}'\) points to stack with \([\text{base}_{\text{stk}} \mapsto 1]\) used and \(ms_{\text{unused}}\) unused
  - for some \(ms_{\text{unused}}\) where \(ms'_{\text{stk}} = [\text{base}_{\text{stk}} \mapsto 1] \uplus ms_{\text{unused}}\).
- \(\text{reg}'(r_{\text{adv}}) = c_{\text{adv}}\)

In order to show the observation part necessary for Lemma \(8\) we use the "\(\text{call}\) works"-Lemma (Lemma \(58\)). Show the following

1. \(ms' : n - k W\)
   Use Lemma \(66\) with
   1.1. \(ms_{f2} \uplus ms_{\text{flag}} : n - k [1 \mapsto \text{sta}(\text{perm}, ms_{f2} \uplus ms_{\text{flag}})]\)
       Lemma \(67\)
   1.2. \(ms_{\text{adv}} \uplus ms_{\text{malloc}} \uplus ms_{\text{link}} : n - k W_{\text{part}}\)
       where
       \[W_{\text{part}} = [0 \mapsto \text{malloc}, 0][2 \mapsto \text{sta}(\text{perm}, ms_{\text{link}})][3 \mapsto \text{malloc}, \text{end}_{\text{adv}}]\]
       This amounts to
       1.2.1. \((n - k - 1, ms_{\text{malloc}}) \in H' 1 W_{\text{part}}\) where \(H'\) is the interpretaion of the \(\text{malloc}, 0\) region. Follows from the malloc specification.
       1.2.2. \((n - k - 1, ms_{\text{adv}}) \in H' \text{malloc} 1 W_{\text{part}}\)
       Can be shown using Lemma \(23\)
       1.2.3. \((n - k - 1, ms_{\text{link}}) \in H' \text{malloc} 1 W_{\text{part}}\)
       This amounts to showing
       1.2.3.1. \((n - k - 2, c_{\text{malloc}}) \in V(W_{\text{part}})\) Follows from Lemma \(50\)
       1.2.3.2. \((n - k - 2, c_{\text{adv}}) \in V(W_{\text{part}})\)
       Follows from Theorem \(2\) using Lemma \(22\)

2. Hyp-Callee
   Assume
   - \(\text{dom}(ms_{\text{unused}}) = \text{dom}(ms_{\text{act}} \uplus ms'_{\text{unused}})\).
\[ W' = \text{revokeTemp}(W)[\text{\texttt{sta}}(\text{temp}, ms_{\text{stk}} \uplus ms_{\text{act}}), \text{\texttt{wul}}(\text{dom}(ms'_{\text{unused}}))], \]

- \[ ms'' : n_{k-1} W' \]
- \[ \text{reg}' \text{ points to stack with } \emptyset \text{ used and } ms'_{\text{unused}} \text{ unused} \]
- \[ \text{reg}' = \text{reg}_{0}[pc \mapsto \text{updatePcPerm}(c_{\text{adv}}), r_{0} \mapsto c_{\text{ret}}, r_{\text{stk}} \mapsto c'_{\text{stk}}, r_{\text{adv}} \mapsto c_{\text{adv}}] \]
- \[ (n - k - 1, c_{\text{ret}}) \in \mathcal{V}(W') \]
- \[ (n - k - 1, c'_{\text{stk}}) \in \mathcal{V}(W') \]

Show
\[ (n - k - 1, (\text{reg}', ms'')) \in \mathcal{O}(W') \]

By Theorem 2 we get
\[ (n - k - 1, \text{updatePcPerm}(c_{\text{adv}})) \in \mathcal{E}(W') \]

getting the desired result amounts to\footnote{We have memory satisfaction by assumption and the above entails the register-file is in the register-file relation.}

2.1. \[ (n - k - 1, c_{\text{adv}}) \in \mathcal{V}(W) \]

To this end let \( n' < n - k - 1 \) and \( W'' \equiv_{\text{priv}} W' \) be given and show
\[ (n', \text{updatePcPerm}(c_{\text{adv}})) \in \mathcal{E}(W'') \]

Follows from Theorem 2 and Lemma 22.

3. Hyp-Cont

Assume

- \[ n' \leq n - 2 \]
- \[ W'' \equiv_{\text{pub}} \text{revokeTemp}(W) \]
- \[ ms'' : n' \text{revokeTemp}(W'') \]
- \[ \text{reg}''(pc) = c_{\text{next}} \]
- \[ \text{reg}'' \text{ points to stack with } ms_{\text{stk}} \text{ used and } ms''_{\text{unused}} \text{ unused for some } ms''_{\text{unused}} \]

and show
\[ (n', (\text{reg}'', ms'' \uplus [base_{\text{stk}} \mapsto 1] \uplus ms''_{\text{unused}})) \in \mathcal{O}(W'') \]

From \[ ms'' : n' \text{revokeTemp}(W'') \], we get that \( ms_{f2} \) is unchanged. Given a frame \( ms'_f \) and assuming \( n' \) is sufficiently large, the execution continues as follows:
\[ (\text{reg}'', ms'' \uplus [base_{\text{stk}} \mapsto 1] \uplus ms''_{\text{unused}}) \rightarrow_k (\text{halted, ms'' \uplus [base_{\text{stk}} \mapsto 1] \uplus ms''_{\text{unused}}}) \]

because 1 is popped off the stack to a register, then it is compared with 1 in the assertion, so the assertion succeeds and halts immediately after.

By assumption we had \( ms'' : n' \text{revokeTemp}(W'') \) which gives us exactly the memory satisfaction required by \( \mathcal{O}(W'') \).

\[ \square \]
let f = fun adv =>
    let l = 1 in
    adv(l);
    l := 1;
    adv(0);
    assert(!l == 1)

In this example let l = 1 in allocates a new local capability l with read-write permissions. Assuming adv has no access to capabilities with permit write local, they cannot store l and thus change its value in the second call.

4.3 Well-Bracketedness Using Local Capabilities and scall

f3: push 1
    fetch r1 adv
    scall r1([],[])
    pop r1
    assert r1 1
    push 2
    fetch r1 adv
    scall r1([],[])
3f: halt

The assertion of f3 may seem a bit awkward because it is between two calls. If an adversary could capture the protected return pointer from the first call and save it until the second call, then the adversary could jump to it again. At this point the top of the stack would be 2, so when the execution reaches the assertion, it would fail. However, the produced return pointer is passed as a local capability, so the only place the adversary can store it is on the stack. The adversary loses control of the stack when control is returned to f3 where the scall makes sure to sanitise the stack and register file before control is passed back to the adversary. In other words, the adversary has no way to capture the continuation which makes the above safe and well-bracketed.

Lemma 4 (Correctness lemma for f3). For all n ∈ ℕ let

\[ c_{adv} \overset{df}{=} ((E, GLOBAL), base_{adv}, end_{adv}, base_{adv} + offsetLinkFlag) \]
\[ c_{f3} \overset{df}{=} ((RWX, GLOBAL), f3 - offsetLinkFlag, 3f, f3) \]
\[ c_{stk} \overset{df}{=} ((RWLX, LOCAL), base_{stk}, end_{stk}, base_{stk} - 1) \]
\[ c_{malloc} \overset{df}{=} ((E, GLOBAL), base_{malloc}, end_{malloc}, base_{malloc} + offsetLinkFlag) \]
\[ c_{link} \overset{df}{=} ((RO, GLOBAL), link, link + 1, link) \]
\[ \text{reg} \in \text{Reg} \]
\[ m \overset{df}{=} ms_{f3} \uplus ms_{flag} \uplus ms_{link} \uplus ms_{adv} \uplus ms_{malloc} \uplus ms_{stk} \uplus ms_{frame} \]

and

- \( c_{malloc} \) satisfies the specification for malloc.
where
\[
\text{dom}(ms_{f3}) = [f3 - \text{offsetLinkFlag}, 3f] \\
\text{dom}(ms_{flag}) = [\text{flag}, \text{flag}] \\
\text{dom}(ms_{link}) = [\text{link}, \text{link} + 1] \\
\text{dom}(ms_{stk}) = [\text{base}_{stk}, \text{end}_{stk}] \\
\text{dom}(ms_{adv}) = [\text{base}_{adv}, \text{end}_{adv}] \\
ms_{malloc} : n[0 \mapsto \iota_{malloc}, 0]
\]

and

- \(ms_{f3}(f3 - \text{offsetLinkFlag}) = ((\text{ro, global}), \text{link}, \text{link} + 1, \text{link}), ms_{f3}(f3 - \text{offsetLinkFlag} + 1) = ((\text{rw, global}), \text{flag}, \text{flag}, \text{flag})\), the rest of \(ms_{f3}\) contains the code of \(f3\).
- \(ms_{flag} = [\text{flag} \mapsto 0]\)
- \(ms_{link} = [\text{link} \mapsto c_{malloc}, \text{link} + 1 \mapsto c_{adv}]\)
- \(ms_{adv}(\text{base}_{adv}) = c_{link} \text{ and all other addresses of } ms_{adv} \text{ contain instructions.}\

if
\[
(reg[pc \mapsto c_{f3}][r_{stk} \mapsto c_{stk}], m) \rightarrow_n (\text{halted}, m'),
\]
then
\[
m'(\text{flag}) = 0
\]

In an attempt to aid the reader, we first provide to high-level descriptions of possible proof of Lemma 4 followed by a more detailed proof.

**Proof of Lemma 4 (high-level description).** Executing \(f2\) until just after the jump in the first scall brings us to a configuration where the stack contains 1 followed by some activation code followed by all zeros. The pc-register contains an executable adversary capability, register \(r_0\) contains a protected return pointer - that is a local enter capability for the execution code, and the \(r_{stk}\) contains a capability for the cleared part of the stack.

At this point we can define a world with permanent regions

- fixing the assertion flag, the code of \(f2\), and the linking table.
- the initial malloc region
- a \(\iota_{nwl,p}\) region

and temporary regions

- a region fixing the private part of the stack
- a \(\iota_{pwl}\) region for the rest of the stack

From the FTLR, we get that in any future world of \(W\), the adversary capability and its executable counter part is in the expression relation and thus safe to execute in suitable configurations. If the configuration we consider right now is suitable, then the execution produces a memory where the permanent invariants of \(W\) are kept which means that the flag is 0.
To argue that the configuration is suitable, we need to argue that invoking the continuation produces an admissible result. As the continuation is a local capability, we take a public future world of $W$. In this public world, the private part of the stack remains the same as before the jump, so when we reach the assertion it succeeds and execution continues. At the point of the jump in the second scall, the stack contains 2 instead of 1, but otherwise essentially the same. Here we again use that it is safe to execute the adversary and that the continuation in this case halts immediately in a configuration where the assertion flag must be 0.

Proof of Lemma $4$ (high-level description 2). If we can show
\[(reg[pc \mapsto c_{f3}][r_{stk} \mapsto c_{stk}], m_{s\text{malloc}} \uplus m_{s\text{stk}} \uplus m_{s\text{adv}} \uplus m_{s\text{stk}}) \in O(W),\]for a world $W$ where the assertion flag is permanently 0, then it is still 0 in any configuration the execution halts in. $W$ also needs to require the program and the linking table to permanently remain the same, have a region that governs malloc and a standard permanent no-write local region for the adversary.

Due to Lemma $58$ the scall lemma, for each scall we have to argue that the adversary and continuation produces results that respect the regions of $W$. Using Lemma $8$ the $O$ anti-reduction lemma, it suffices to argue that each part of $f_{3}$ between scalls produces admissible results.

Executing until the first scall only pushes 1 to the stack, so the invariants of $W$ are preserved. Due to the scall lemma, we need to argue that that the adversary and the continuation produce admissible results.

Using the FTLR, we get that the executable capability for the adversary is in the $E$-relation. As we provide no arguments to the adversary, most of the conditions are satisfied by assumptions and Lemma $62$ which makes sure that the stack capability is in the value relation. Which gives us that the adversary produces an admissible result.

With respect to the continuation, it is passed to the adversary as a local capability, so when we reason about it, we consider public future worlds. The scall uses temporary regions for the stack and these persist in public future worlds. This allows us to assume that the private part of the stack still contains 1 after the call. Further, the program, flags, and linking table remain the same in any kind of future world. Therefore, we know that the execution continues by popping 1 from the stack and then asserting that it is indeed 1, which is indeed the case, so 2 is pushed to the stack. At this point we reach another scall. No changes where made to the permanent part of the stack, so the invariants are still satisfied. At this point we use the scall lemma one last time. The adversary call code is well-behaved for the same reasons as in the first call. The scall lemma lets us assume that the continuation continues in a memory that satisfies the invariants of $W$. The execution halts immediately in the continuation, so it produces an admissible result.

Proof of Lemma $4$. Assume the premises of the lemma. Now define
\[
W = [0 \mapsto t_{\text{malloc}, 0}]
[1 \mapsto t_{\text{str}, (\text{perm}, m_{s\text{flag}} \uplus m_{s\text{f2}})}]
[2 \mapsto t_{\text{str}, u}(\text{perm}, m_{s\text{link}})]
[3 \mapsto t_{\text{nostr}}(\text{base}_{adv}, \text{end}_{adv})]
\]

Further define
\[
m'_{s} = m_{s\text{flag}} \uplus m_{s\text{f2}} \uplus m_{s\text{link}} \uplus m_{s\text{adv}}
\]
If we can show
\[(n + 1, (\text{reg} | pc \mapsto c_{f3}) [r_{stk} \mapsto c_{stk}], ms_{malloc} \uplus ms' \uplus ms_{adv} \uplus ms_{stk}) \in \mathcal{O}(W),\]
then using \(ms_{frame}\) as the frame and \(m'\) as the resulting memory, we get that \(m' = ms'' \uplus ms_r \uplus ms_{frame}\) for some \(ms'\) and \(ms_r\) s.t. \(ms'' : 1 W\). Region 1 guarantees that the assertion flag is unchanged, so we have
\[m'(\text{flag}) = 0\]
So SFTS 3. To do so, we use Lemma 8. Let \(ms_f\) be given. The execution proceeds as follows:
\[(\text{reg} | pc \mapsto c_{f3}) [r_{stk} \mapsto c_{stk}], ms' \uplus ms_{stk} \uplus ms_f) \rightarrow_i (\text{reg}', ms' \uplus [\text{base}_{stk} \mapsto 1] \uplus ms_{stk}|_{\text{base}_{stk}+1, \text{end}_{stk}} \uplus ms_f),\]
where
\[(\text{reg}', ms')\) is looking at \texttt{scall r([[], []])} followed by \texttt{cnext}\]
where \(\texttt{cnext}\) is \(c_{f3}\) adjusted to point to the next instruction, namely \texttt{pop r1}. Further we have
- \(\text{reg}'\) points to stack with \([\text{base}_{stk} \mapsto 1]\) used and \(ms_{stk}|_{\text{base}_{stk}+1, \text{end}_{stk}}\) unused
and \(i\) is a suitable number of steps.
To show
\[(n - i, (\text{reg}', ms' \uplus [\text{base}_{stk} \mapsto 1] \uplus ms_{stk}|_{\text{base}_{stk}+1, \text{end}_{stk}})) \in \mathcal{O}(W)\]
We use Lemma 58 (we do not use the local frame in the lemma) which requires us to show

1. \(ms' : n-i W\)
   Partition \(ms'\) as follows:
   1.1. \(ms_{malloc}:\) governed by \(\iota_{malloc, 0}\), use malloc specification.
   1.2. \(ms_{flag} \uplus ms_f:\) governed by region 1, only this memory segment is accepted.
   1.3. \(ms_{link}:\) governed by region 2, only this memory segment is accepted. We also need to show that the contents is safe, i.e. shoe
   1.3.1. \((n - i, c_{malloc}) \in \mathcal{V}(W):\) Follows from Lemma 50
   1.3.2. \((n - i, c_{adv}) \in \mathcal{V}(W):\)
       We will show
       \[\forall W' \sqsupseteq_{\text{priv}} W, (n, c_{adv}) \in \mathcal{V}(W')\]
       which will give us what we need using downwards closure as well as a result for later use.
       Let \(W' \sqsupseteq_{\text{priv}} W\) be given and show
       \[(n, (\text{base}_{adv}, \text{end}_{adv}, \text{base}_{adv} + \text{offsetLinkFlag}) \in \text{enterCondition}(\text{GLOBAL})(W')\]
       to this end let \(W'' \sqsupseteq_{\text{priv}} W'\) and \(n' < n\) be given and show
       \[(n', \text{updatePcPerm}(c_{adv})) \in \mathcal{E}(W'')\]
       This follows from the FTLR (Theorem 2) if we can show
       \[(n', \text{base}_{adv}, \text{end}_{adv}) \in \text{readCondition}(\text{GLOBAL})(W'')\]
       \(\iota_{\text{pewl}, p\overline{\text{base}}_{adv}, \text{end}_{adv}}\) governs the adversary, so the result follows from Lemma 22
1.4. \( ms_{adv} \): Follows from Lemma 23.

2. Hyp-Callee

Assume

- \( \text{dom}(ms_{stk}|_{base_{stk}+1,end_{stk}}) = \text{dom}(ms_{act} \uplus ms'_{unused}) \)
- \( W' = \text{revokeTemp}(W)[l^{\text{sta}}(\text{temp}, [base_{stk} \mapsto 1] \uplus ms_{act}), l^{\text{pw}}(\text{dom}(ms'_{unused}))] \)
- \( ms'' : n-i-1 \)
- \( \text{reg''} \) points to stack with \( \emptyset \) used and \( ms'_{unused} \) unused
- \( reg'' = \text{reg}_0[pc \mapsto \text{updatePcPerm}(reg'(r)), r_0 \mapsto c_{ret}, r_{stk} \mapsto c'_{stk}, r \mapsto reg'(r)] \)
- \( (n-i-1,c_{ret}) \in \mathcal{V}(W') \)
- \( (n-i-1,c'_{stk}) \in \mathcal{V}(W') \)

for some \( ms_{act}, ms_{unused}, ms'', reg'', c_{ret} \).

Using the FTLR, we get \( (n-i-1, updatePcPerm(c_{adv})) \in \mathcal{E}(W') \), from

2.1. \( ms'' : n-i-1 \)

2.2. \( (n-i-1, reg'') \in \mathcal{V}(W') \):

show

2.2.1. \( (n-i-1,c_{ret}) \in \mathcal{V}(W') \) : by above assumptions.
2.2.2. \( (n-i-1,c'_{stk}) \in \mathcal{V}(W') \) : by above assumptions.
2.2.3. \( (n-i-1,c_{adv}) \in \mathcal{V}(W') \) : follows from 4.
2.2.4. The remaining registers we need to consider contain 0 and are thus trivial to show.

we get

\( (n-i-1,(ms'', reg'')) \in \mathcal{O}(W') \)

3. Hyp-Cont

Assume:

- \( n' \leq n-i-2 \)
- \( W'' \geq pub \text{revokeTemp}(W) \)
- \( ms' : n' \text{revokeTemp}(W'') \)
- for all \( r \), we have that:

\[
\text{reg''}(r) = \begin{cases} 
\text{c}_{next} & \text{if } r = pc \\
\in \mathcal{V}(W'') & \text{if } \text{reg''}(r) \text{ is a global capability and } r \notin \{pc,r_{stk}\}
\end{cases}
\]

- \( \text{reg''} \) points to stack with \( [base_{stk} \mapsto 1] \) used and \( ms'_{unused} \) unused for some \( ms''_{unused} \)

and show

3.1. \( (\text{reg''}, ms'' \uplus [base_{stk} \mapsto 1] \uplus ms''_{unused}) \in \mathcal{O}(\text{revokeTemp}(W'')) \)

As \( W'' \geq pub W \), we know that the program, assertion flag, and linking table remain unchanged in \( ms'' \). Given some frame \( ms' \), then the execution proceeds by first succeeding the assertion and then pushing 2 to the stack:

\( (\text{reg''}, ms'' \uplus [base_{stk} \mapsto 1] \uplus ms''_{unused} \uplus ms'_f) \rightarrow_k (\text{reg'}^{(3)}, ms'' \uplus [base_{stk} \mapsto 2] \uplus ms''_{unused} \uplus ms'_f) \)

where
3.1.1. $\text{Hyp-Callee}$

By Lemma 8 it suffices to show

3.1.1.2. $\text{Hyp-Cont}$

3.1.1.2.2. $\text{Hyp-Cont}$ is satisfied by one of the first Hyp-cont assumptions and Lemma 47.

3.1.1.2.2.1. $\text{Hyp-Cont}$ is looking at $\text{scall } r([], [])$ followed by $c'_{\text{next}}$

3.1.1.2.2.2. $\text{Hyp-Cont}$ is a global capability and $r \not\in \{\text{pc}, r_{\text{stk}}\}$

3.1.1.2.2.3. $\text{Hyp-Cont}$ is a global capability and $r \not\in \{\text{pc}, r_{\text{stk}}\}$

By Lemma 8 it suffices to show

3.1.1.1. $\{n' - k, (\text{reg}^{(3)}, \text{ms}'' | [\text{base}_{\text{stk}} \mapsto 2] \models \text{ms}''_{\text{unused}})\} \in \mathcal{O}(\text{revokeTemp}(W''))$

Show this using Lemma 58.a. Show:

3.1.1.2. Hyp-Callee

Assume:

- $\text{dom}(\text{ms}''_{\text{unused}}) = \text{dom}(\text{ms}'_{\text{act}} \uplus \text{ms}^{(3)}_{\text{unused}})$
- $W^{(3)} = \text{revokeTemp}(W'')[\text{sta}(\text{temp}, [\text{base}_{\text{stk}} \mapsto 2]|\text{ms}'_{\text{act}}, r_{\text{adv}}(\text{dom}(\text{ms}^{(3)}_{\text{unused}})))]$
- $\text{ms}^{(3)} : n' - k - 1 W^{(3)}$
- $\text{reg}^{(4)}$ points to stack with $\emptyset$ used and $\text{ms}^{(3)}_{\text{unused}}$ unused
- $\text{reg}^{(4)} = \text{reg}^{(4)}[\text{pc} \mapsto \text{updatePcPerm}(c_{\text{adv}}), r_0 \mapsto c'_{\text{ret}}, r_{\text{stk}} \mapsto c''_{\text{stk}}, r \mapsto c_{\text{adv}}]$
- $(n' - k - 1, c'_{\text{ret}}) \in \mathcal{V}(W^{(3)})$
- $(n' - k - 1, c''_{\text{stk}}) \in \mathcal{V}(W^{(3)})$

This argument is almost identical to the one we just did for the first call: Using the FTLR, we get $(n - i - 1, \text{updatePcPerm}(c_{\text{adv}})) \in \mathcal{E}(W^{(3)})$. Which we use with

3.1.1.2.1. $\text{ms}^{(3)} : n' - k - 1 W^{(3)}$: By assumption.

3.1.1.2.2. $(n' - k - 1, \text{reg}^{(4)}) \in \mathcal{R}(W^{(3)})$: Show:

3.1.1.2.2.1. $(n' - k - 1, c_{\text{adv}}) \in \mathcal{V}(W^{(3)})$ by Assumption 4.

3.1.1.2.2.2. $(n' - k - 1, c'_{\text{ret}})$ by assumption.

3.1.1.2.2.3. $(n' - k - 1, c''_{\text{stk}})$ by assumption to get

$$\left(n' - k - 1, (\text{reg}^{(4)}, \text{ms}^{(3)})\right) \in \mathcal{O}(W^{(3)})$$

3.1.1.3. Hyp-Cont

Assume

- $n'' \leq n' - k - 2$
- $W^{(3)} \sqsupset^{\text{pub}} \text{revokeTemp}(W'')[\text{sta}(\text{temp}, \text{ms}_{\text{stk}})] [\text{sta}(\text{temp}, \text{ms}^{(3)}_{\text{unused}})]$
- $\text{ms}^{(3)} : n'' \text{revokeTemp}(W^{(3)})$
- for all $r$, we have that:

$$\text{reg}^{(4)}(r) \begin{cases} = r'_{\text{next}} & \text{if } r = \text{pc} \\ \in \mathcal{V}(W'') & \text{if } \text{reg}^{(4)}(r) \text{ is a global capability and } r \not\in \{\text{pc}, r_{\text{stk}}\} \end{cases}$$

- $\text{reg}'$ points to stack with $[\text{base}_{\text{stk}} \mapsto 2]$ used and $\text{ms}^{(3)}_{\text{unused}}$ unused for some $\text{ms}^{(3)}_{\text{unused}}$

and show

$$\left(n'', (\text{reg}^{(3)}, \text{ms}^{(3)} \uplus [\text{base}_{\text{stk}} \mapsto 2] \uplus \text{ms}^{(3)}_{\text{unused}})\right) \in \mathcal{O}(\text{revokeTemp}(W^{(3)}))$$

3.1.1.3.
To this end let $ms''', m''$, and $j \leq n''$ be given and assume

$$(\text{reg}^{3}, ms^{3} ⊔ [\text{base}_{\text{stk}} \mapsto 2] ⊔ ms''_{\text{unused}} ⊔ ms''_{\text{f}}) \rightarrow j (\text{halted}, m'')$$

As the execution halts immediately,

$$m'' = ms^{3} ⊔ [\text{base}_{\text{stk}} \mapsto 2] ⊔ ms''_{\text{unused}} ⊔ ms''_{\text{f}}$$

By assumption we had $ms^{3} :_{w''} \text{revokeTemp}(W^{3})$ and the frame is unchanged, so we can split the memory as needed.

\[\square\]

### 4.4 Inverted Control and Return From Closure

The following example is constructed to investigate the difficulties of preserving an adversary’s local frame. There is no assertion as this is (slightly) beside the point. The lemma we would prove about this should look like Lemma \[\text{Lemma 5}\] but it is not state and proven here.

The assembly code is as follows:

```assembly
4.4 Inverted Control and Return From Closure

The following example is constructed to investigate the difficulties of preserving an adversary’s local frame. There is no assertion as this is (slightly) beside the point. The lemma we would prove about this should look like Lemma \[\text{Lemma 5}\] but it is not state and proven here.

4.5 Variant of the “awkward” example

Assembly variant of the “awkward” example from Dreyer et al., 2010, p. 11 which roughly was:

```
g = fun _ => let x = 0 in
    fun f =>
        x := 0;
        f();
        x := 1;
        f();
        assert(x == 1)
```

Our translation of the example:

```assembly
4.5 Variant of the “awkward” example

Assembly variant of the “awkward” example from Dreyer et al., 2010, p. 11 which roughly was:

```
g = fun _ => let x = 0 in
    fun f =>
        x := 0;
        f();
        x := 1;
        f();
        assert(x == 1)
```

Our translation of the example:

```
g1: malloc r2 1
    store r2 0
    move r3 pc
    lea r3 ...
    crate \(\{(x, r2)\}\) r3
    rclear RegisterName \{pc, r0, r1\}
    g2: move r3 pc
        lea r3 ...
        crate \(\{\}\) r3
        rclear RegisterName \{pc, r0, r1\}
        2g: jmp r0
        f5: reqglob r1
            prepstack rstk
            sall r1(\(\{\}\, [r0, r_{\text{env}}]\))
            mclear rstk
            rclear RegisterName \{r0, pc\}
        5f: jmp r0
```

38
1g: jmp r₀

4f: regglob r₁
    prepstack r stk
    store x 0
    scall r₁([[], [r₀, r₁, r env]])
    store x 1
    scall r₁([[], [r₀, r env]])
    load r₁ x
    assert r₁ 1
    mclear r stk
    rclear RegisterName \ {r₀, pc}

4f: jmp r₀

Where the ... is the appropriate offset to make the capability point to f₄.

Lemma 5 (Correctness of g₁). For all n ∈ N let

\[ c_{adv} \overset{\text{def}}{=} ((\text{RWX, GLOBAL}), \text{base}_{adv}, \text{end}_{adv}, \text{base}_{adv} + \text{offsetLinkFlag}) \]
\[ c_{g₁} \overset{\text{def}}{=} ((\text{E, GLOBAL}), g₁ - \text{offsetLinkFlag}, 4f, g₁) \]
\[ c_{stk} \overset{\text{def}}{=} ((\text{RWX, LOCAL}), \text{base}_{stk}, \text{end}_{stk}, \text{base}_{stk} - 1) \]
\[ c_{malloc} \overset{\text{def}}{=} ((\text{E, GLOBAL}), \text{base}_{malloc}, \text{end}_{malloc}, \text{base}_{malloc} + \text{offsetLinkFlag}) \]
\[ c_{link} \overset{\text{def}}{=} ((\text{RO, GLOBAL}), \text{link}, \text{link}, \text{link}) \]
\[ m \overset{\text{def}}{=} ms_{g₁} \uplus ms_{flag} \uplus ms_{link} \uplus ms_{adv} \uplus ms_{malloc} \uplus ms_{stk} \uplus ms_{frame} \]

where

- \( c_{malloc} \) satisfies the specification for malloc with \( \iota_{malloc, 0} \)

\[
\begin{align*}
\text{dom}(ms_{g₁}) &= [g₁ - \text{offsetLinkFlag}, 4f] \\
\text{dom}(ms_{flag}) &= [\text{flag}, \text{flag}] \\
\text{dom}(ms_{link}) &= [\text{link}, \text{link}] \\
\text{dom}(ms_{stk}) &= [\text{base}_{stk}, \text{end}_{stk}] \\
\text{dom}(ms_{adv}) &= [\text{base}_{adv}, \text{end}_{adv}] \\
ms_{malloc} \colon n \mapsto \iota_{malloc, 0}
\end{align*}
\]

and

- \( ms_{g₁}(g₁ - \text{offsetLinkFlag}) = ((\text{RO, GLOBAL}), \text{link}, \text{link}, \text{link}), ms_{g₁}(g₁ - \text{offsetLinkFlag} + 1) = ((\text{RW, GLOBAL}), \text{flag}, \text{flag}, \text{flag}) \), the rest of \( ms_{g₁} \) contains the code of \( g₁ \) immediately followed by the code of \( f₄ \).
- \( ms_{flag} = [\text{flag} \mapsto 0] \)
- \( ms_{link} = [\text{link} \mapsto c_{malloc}] \)
- \( ms_{adv}(\text{base}_{adv}) = c_{link} \) and all other addresses of \( ms_{adv} \) contain instructions.
- \( \forall a \in \text{dom}(ms_{stk}), ms_{stk}(a) = 0 \)
if 
\[(\text{reg}_0[\text{pc} \mapsto c_{adv}][r_{stk} \mapsto c_{stk}][r_1 \mapsto c_{g_1}], m) \rightarrow_n (\text{halted}, m')\],
then
\[m'(\text{flag}) = 0\]

In the proof of Lemma 5, we will use the following region

Definition 2.
\[\iota_x = (\text{perm}, 0, \phi_{pub}, \phi, H_x)\]
\[\phi_{pub} = \{(0, 1)\}^*\]
\[\phi = (1, 0) \cup \phi_{pub}\]
\[H_x s W = \{(n, ms) | ms(x) = s \land n > 0\} \cup \{(0, ms)\}\]

Lemma 6. Definition 2 defines a region.

Proof of Lemma 6.

• \(\phi_{pub}\) is defined as the reflexive transitive closure, so it is immediately well formed.
• \(\phi\) adds a transition to \(\phi_{pub}\) and is also reflexive and transitive.
• \(H_x\) is trivially non-expansive in the state.
• \(H_x\) does not depend on the \(W\), so it also becomes trivially non-expansive and (privately) monotone in \(W\).

Proof of Lemma 5 (using call lemma).

Let \(n\) be given and make the assumptions of the lemma. Define
\[W = [0 \mapsto \iota_{\text{malloc,0}}]
[1 \mapsto \iota_{\text{sta,0}}(\text{perm}, ms_{\text{link}})]
[2 \mapsto \iota_{\text{pwl,0}}(\text{perm}, ms_{\text{link}})]
[3 \mapsto \iota_{\text{nwl,0}}(\text{perm}, ms_{\text{link}})]
[4 \mapsto \iota_{\text{sta,0}}(\text{perm}, ms_{\text{link}})]\]

and
\[ms = ms_{g_1} \oplus ms_{\text{flag}} \oplus ms_{\text{link}} \oplus ms_{\text{adv}} \oplus ms_{\text{malloc}}\]

If we can show
\[(n, (\text{reg}_0[\text{pc} \mapsto c_{adv}][r_{stk} \mapsto c_{stk}][r_1 \mapsto c_{g_1}], ms \oplus ms_{\text{stk}})) \in \mathcal{O}(W)\] (5)
then the termination assumption gives us that part of \(m\) satisfies a private future world of \(W\).
Region 4 is permanent, so
\[m(\text{flag}) = 0\]
So it suffices to show Eq. 5. To this end use the FTLR to show \((n, c_{adv}) \in \mathcal{E}(W)\), so show
1. \((n, (\text{base}_{adv}, \text{end}_{adv})) \in \text{readCondition} (\text{GLOBAL})(W)\)
   Simple using region 3 in \(W\) and Lemma 22.

2. \((n, (\text{base}_{adv}, \text{end}_{adv})) \in \text{writeCondition} (\text{nwl}, \text{GLOBAL})(W)\)
   Simple using region 3 in \(W\), using Lemma 15.

In conclusion \((n, c_{adv}) \in \mathcal{E}(W)\). We get Eq. 5 if we show 3. and 4.:

3. \(m_{s} \sqcup m_{stk} : n W\)
   3.1. \(m_{sg} \sqcup m_{flag} : n [4 \mapsto \iota \text{sta}(\text{perm}, m_{sg} \sqcup m_{flag})]\)
   Lemma 67.
   3.2. \(m_{stk} : n [2 \mapsto \iota \text{pwl}_{\text{base}_{stk}, \text{end}_{stk}}]\)
   Lemma 68 and assumption that \(m_{stk}\) is all 0.
   3.3. \(m_{malloc} \sqcup m_{link} \sqcup m_{adv} : n [0 \mapsto \iota \text{malloc}, 0][1 \mapsto \iota \text{sta}_{\text{u}}(\text{perm}, m_{link})][3 \mapsto \iota \text{nwl}_{\text{p}, \text{end}_{adv}}]\)
   For convenience define
   \[W_{\text{mini}} = [0 \mapsto \iota \text{malloc}, 0][1 \mapsto \iota \text{sta}_{\text{u}}(\text{perm}, m_{link})][3 \mapsto \iota \text{nwl}_{\text{p}, \text{end}_{adv}}]\]
   Partitioning the memory segment in the components of the disjoint union, the \text{malloc}
   part follows from assumption \(m_{malloc} : n [0 \mapsto \iota \text{malloc}, 0]\) and the \text{malloc}
   specification. The linking table part of memory amounts to showing:
   \[(n, m_{link}) \in H^{\text{sta}_{u}(m_{link})}(1)(\xi^{-1}(W_{\text{mini}}))\]
   which in turn amounts to showing
   \[(n - 1, c_{malloc}) \in \mathcal{V}(W_{\text{mini}})\]
   which follows from Lemma 50.
   Showing
   \[(n, m_{adv}) \in H^{\text{sta}_{\text{base}_{adv}, \text{end}_{adv}}}(1)(\xi^{-1}(W_{\text{mini}}))\]
   is a bit more involved. It amounts to
   \[\forall a \in \text{dom}(m_{adv}). (n - 1, m_{adv}(a)) \in \mathcal{V}(W_{\text{mini}})\]
   which in turn is trivial for everything but
   \[(n - 1, c_{link}) \in \mathcal{V}(W_{\text{mini}})\]
   This amounts to showing
   \[(n - 1, (\text{link}, \text{link})) \in \text{readCondition} (\text{GLOBAL})(W_{\text{mini}})\]
   which amounts to
   \[\iota \text{sta}_{\text{u}}(\text{perm}, m_{link}) \overset{n-1}{\subseteq} \iota \text{nwl}_{\text{link}, \text{link}}\]
   which follows from Lemma 23.

Using Lemma 66 repeatedly with 3.1., 3.2., and 3.3. gives the desired memory satisfaction.
4. \((n, reg_0[r_{stk} \mapsto c_{stk}] | r_1 \mapsto c_{g1}) \in \mathcal{R}(W)\)

This amounts to showing

4.1. \((n, reg_0[r_{stk} \mapsto c_{stk}] | r_1 \mapsto c_{g1}(c_{stk})) \in \mathcal{V}(W)\)

The assumptions on \(c_{stk}\) and \(ms_{stk}\) in the lemma entail

- \(reg_0[r_{stk} \mapsto c_{stk}] | r_1 \mapsto c_{g1}\) points to stack with \(\emptyset\) used and \(ms_{stk}\) unused

and further there is a \(\text{perm}^{\emptyset}\) region for \(ms_{stk}\) in \(W\), so the result follows from Lemma 62

4.2. \((n, c_{g1}) \in \mathcal{V}(W)\)

Let \(n_1 < n\) and \(W_1 \supseteq \text{priv} W\) and show

\[(n_1, \text{updatePcPerm}(c_{g1})) \in \mathcal{E}(W_1)\]

To this end assume \(n_2 \leq n_1\), \(ms_1 : n_2 W_1\), and \((n_2, reg_1) \in \mathcal{R}(W_1)\) and show

\[(n_2, (reg_1[pc \mapsto \text{updatePcPerm}(c_{g1})], ms_1)) \in \mathcal{O}(W_1)\]

Using Lemma 59, Lemma 60, Lemma 8 (and some others), it suffices to show

\[(n'_2, (reg_2, ms_2 \uplus ms'_{malloc} \uplus ms_{cls} \uplus ms_{x})) \in \mathcal{O}(W_2)\]

where

\[W_2 = W_1[0 \mapsto \tau_{malloc}[i_1 \mapsto \tau_{sta}(perm, ms_{cls})][i_2 \mapsto \tau_x] \]

where \(i_1, i_2 \notin \text{dom}(W_1)\) and \(i_1 \neq i_2\) and \(\tau_x\) is the region in Definition 2 which is a region by Lemma 62. Also

- \(\tau_{malloc} \supseteq \text{priv} \tau'_{malloc}\)
- \(c_x = ((\text{RWX}, \text{GLOBAL}), x, x, x)\)
- \(ms_x = [x \mapsto 0]\)
- \(ms_2 \uplus ms'_{malloc} \uplus ms_{cls} \uplus ms_x \uplus n_2^{-1} W_2\)
- \(c_{env} = ((\text{RWX}, \text{GLOBAL}, env, env, env))\)
- \(ms_{env} = [env \mapsto c_x]\)
- \(c_{f4} = ((\text{RWX}, \text{GLOBAL}), g1 - \text{offsetLinkFlag}, 4f, f4)\)
- \(ms_{cls} = ms_{env} \uplus ms_{act}\)

Finally assume Hyp-Act:

\[{\forall \text{reg}, ms, \text{reg}(pc) = c_{cls} \Rightarrow}
\exists j. \forall ms_f. (\text{reg}, ms \uplus ms_{cls} \uplus ms_f) \rightarrow_j (\text{reg}[pc \mapsto \text{updatePcPerm}(c_{f4})][r_{env} \mapsto c_{env}], ms \uplus ms_{cls} \uplus ms_f)\]  \hspace{1cm} (6)

Show

\[(n_2 - i, (reg_2, ms_2 \uplus ms'_{malloc} \uplus ms_{env} \uplus ms_x \uplus ms_{cls})) \in \mathcal{O}(W_2)\]  \hspace{1cm} (7)

If \(\text{reg}_1(r_0).\text{perm} \notin \{\text{E, RX, RWX, RWLX}\}\), then the execution fails after the jump and is thus trivially true.

42
If $reg_1(r_0).perm \in \{E, RX, RWX, RWLX\}$, then either `executeCondition` or `enterCondition` holds for the capability in $reg_1(r_0)$. Now use $W_2 \equiv_{pub} W_1$ with the appropriate condition to get

$$(n_2 - i, updatePcPerm(reg_1(r_0))) \in E(W_2)$$

which in turn gives us \([4, 2]\) if we can show the following

4.2.1. $ms_2 \uplus ms'_malloc \uplus ms_{env} \uplus ms_x \uplus ms_{cls} : n_2 - i, W_2$

We first show the following:

- $ms_2 \uplus ms'_malloc : n_2 - i, W_1[0 \mapsto t_{malloc}]$: we already know this.
- $ms_{env} \uplus ms_{cls} : n_2 - i, [i_1 \mapsto \epsilon_{stack}(perm, ms_{env} \uplus ms_{cls})]$: By Lemma 87.
- $ms_x : n_2 - i, t_2 \mapsto t_x$: $ms(x) = 0$, so okay.

4.2.2. $(n_2 - i, reg_2) \in \mathcal{R}(W_2)$

Amounts to showing

4.2.2.1. $(n_2 - i, reg_2(r_0)) \in \mathcal{V}(W_2)$ by assumption $(n_2, reg_1) \in \mathcal{R}(W_1)$ and $\mathcal{V}$ monotonicity wrt. $\equiv_{pub}$

4.2.2.2. $(n_3 - i, c_{cls}) \in \mathcal{V}(W_2)$

Let $n_3 < n_2 - i$ and $W_3 \equiv_{prev} W_2$ be given and show

$$(n_3, updatePcPerm(c_{cls})) \in E(W_3)$$

To this end let $n_4 \leq n_3$, $ms_3 : n_4$, $W_3$, and $(n_4, reg_3) \in \mathcal{R}(W_3)$ and show

$$(n_4, (reg_3[pc \mapsto updatePcPerm(c_{cls})], ms_3)) \in O(W_3) \quad (8)$$

Let $ms'_3$ and $ms_4^j$ be memory segments such that $ms_3 = ms'_3 \uplus ms_4^j$ and $ms_3 : n_4$, `revokeTemp(W_3)` (using Lemma 64). By $ms_3 : n_4$, $W_3$ and $W_3 \equiv_{prev} W_2$, we know $ms_{cls} \subseteq ms'_3$, so using Hyp-Act[4], we get $j$ such that

$$\forall ms_f. (reg_3[pc \mapsto updatePcPerm(c_{cls})], ms'_3 \uplus ms_4^j \uplus ms_f) \mapsto_j (reg_3[pc \mapsto updatePcPerm(c_{cls})][r_{env} \mapsto c_{env}], ms'_3 \uplus ms_4^j \uplus ms_f) \quad (9)$$

Using Lemma 8 it suffices to show

$$(n_4, (reg_3[pc \mapsto updatePcPerm(c_{cls})][r_{env} \mapsto c_{env}], ms'_3 \uplus ms_4^j)) \in O(W_3)$$

Use Lemma 8 again. This time let $ms''_f$ be given and take $ms_x$ to be the part of $ms_3$ that $reg_3(r_{stk})$ does not govern. By the operational semantics, we know

$$(reg_3[pc \mapsto updatePcPerm(c_{cls})][r_{env} \mapsto c_{env}], ms'_3 \uplus ms_4^j \uplus ms''_f) \mapsto_{j'} (reg_4, ms_4 \uplus ms''_f)$$

where

- $(reg_4, ms_4)$ is looking at `call r_1([], [r_0, r_1, r_{env}])` followed by $c_{next}$
  - $c_{next}$ is the capability pointing to the next instruction.
- $(reg_4)$ points to stack with $\emptyset$ used and $ms_{unused} \uplus ms_{unused}$ unused
- `prestack` did not fail, so the stack capability must be RWLX and follow the stack convention.

\[\text{the execution may fail, but then the configuration is trivially in the observation relation.}\]
• $\text{reg}_4(r_1)$ is a GLOBAL capability.
  - $\text{regglob}$ did not fail
• $ms_4(x) = 0$
• $reg_4(r_{\text{env}}) = c_{\text{env}}$
region $i_2$ (the $\iota_2$ region) can be in either state 0 or 1, so to make sure it is in state 0, we use a private transition. So let $W_4$ be $\text{revokeTemp}(W_3)$ with region $i_2$ in state 0. We then have

$$ms_4 :_{n_4-j-j'} W_4$$

Now we can use Lemma 55 to show:

$$(n_4 - j - j', (\text{reg}_4, ms_4 \cup ms_r \cup \emptyset \cup ms_{\text{unused}})) \in O(W_4)$$

where $ms_r$ is the local frame of the scall lemma.

4.2.2.1. $ms_4 :_{n_4-j-j'} \text{revokeTemp}(W_4)$: follows from $W_4 = \text{revokeTemp}(W_4)$

4.2.2.2. Hyp-Callee

We know $(n_4, \text{reg}_3(r_1)) \in V(W_3)$. If this is not a capability that becomes executable when jumped to, then the execution fails, so the register memory segment pair is trivially in the observation relation. If it is executable, then either the executeCondition or the enterCondition holds for appropriate values. We also know that it is a global capability, so we can use it with private future worlds. We have $W_5 = \text{revokeTemp}(W_4)[\alpha^{\text{ste}}(\text{temp}, \emptyset \cup ms_{\text{act}} \cup ms_r, \emptyset_{\text{dom}}(ms_{\text{unused}}))] \supseteq^{\text{priv}} W_3$, for some $ms_{\text{act}}$ and $ms_{\text{unused}}$

By the execute/enter condition, we have

$$(n_4 - j - j', \text{updatePcPerm}(\text{reg}_3(r_1))) \in E(W_5)$$

Now it suffices to show

4.2.2.2.1. $ms_5 :_{n_4-j-j'-1} W_5$ for some $ms_5$ which is one of the assumptions of Hyp-Callee.

4.2.2.2.2. $(n_4 - j - j' - 1, \text{reg}_3) \in R(W_5)$ where $\text{reg}_3$ is as described in the scall lemma Hyp-callee premise.

Amounts to showing:

1) $(n_4 - j - j' - 1, \text{reg}_3(r_1)) \in V(W_5)$, use Lemma 79 with $(n_4 - j - 1, \text{reg}_3(r_1)) \in V(W_3)$, the capability is global, and $W_5 \supseteq^{\text{priv}} W_3$. 2) The protected return pointer and the stack capability are in the value relation by Hyp-callee assumptions.

which gives us

$$(n_4 - j - j' - 1, (\text{reg}_5, ms_5)) \in O(W_5)$$

4.2.2.3. Hyp-Cont

Assume

• $n_5 \leq n_4 - j - j' - 2$
• $W_6 \supseteq^{\text{pub}} \text{revokeTemp}(W_4)$
• $ms_6 :_{n_5} \text{revokeTemp}(W_6)$
• $\text{reg}_5(\text{pc}) = c_{\text{next}}, \text{reg}_6(r_0) = \text{reg}_3(r_0), \text{reg}_6(r_1) = \text{reg}_3(r_1), \text{reg}(r_{\text{env}}) = c_{\text{env}}$
\[\text{reg}_6 \text{ points to stack with } \emptyset \text{ used and } ms''_{\text{unused}} \text{ unused} \]

Show
\[ (n_5, (\text{reg}_6, ms_6 \cup ms_r \cup \emptyset \cup ms''_{\text{unused}})) \in O(W_6) \]

Use the \(O\)-anti-reduction lemma (Lemma 8) followed by the \texttt{scall} lemma (Lemma 58). Given \(ms''_f\), we know by the operational semantics and the fact that the program hasn’t changed that

\[ (\text{reg}_6, ms_6 \cup ms_r \cup ms''_{\text{unused}} \cup ms''_{f}) \rightarrow_k (\text{reg}_7, ms_6[x \mapsto 1] \cup ms_r \cup ms''_{\text{unused}} \cup ms''_{f}) \]

where
\[ \text{reg}_7, ms_6[x \mapsto 1] \]

is looking at \texttt{scall} \(([], [r_0, r_{\text{env}}])\) followed by \(c'_{\text{next}}\)

\[ c'_{\text{next}} \text{ is the current pc capability but looking at load } r_1 x. \]

In \texttt{revokeTemp}(W_6), we don’t know which state the \(i_x\) region is in, but state 1 is reachable via a public transition, so let \(W_7\) be \texttt{revokeTemp}(W_6) with region \(i_2\) in state 1. It follows easily that

\[ ms_6[x \mapsto 1] \vdash_{n_5 - k} W_7 \]

We continue the proof in item 5.

5. At this point, we apply the \texttt{scall} lemma, to get

\[ (n_5 - k, (\text{reg}_7, ms_6[x \mapsto 1] \cup ms_r \cup ms''_{\text{unused}})) \in O(W_7) \]

show

5.1. \(ms_6[x \mapsto 1] \vdash_{n_5 - k} \texttt{revokeTemp}(W_7)\), follows from \(W_7 = \texttt{revokeTemp}(W_7)\).

5.2. Hyp-Callee: Goes like the first Hyp-Callee \([4.2.2.2.2]\).

5.3. Hyp-Cont

Assume:

- \(n_6 \leq n_5 - k - 2\)
- \(W_8 \sqsupseteq_{\text{pub}} \texttt{revokeTemp}(W_7)\)
- \(ms_7 \vdash_{i_8} \texttt{revokeTemp}(W_8)\)
- \(reg_8(r_0, r_{\text{env}}) = reg_7(r_0, r_{\text{env}})\)
- \(reg_8(pc) = c'_{\text{next}}\)
- \(reg_8\) points to stack with \(\emptyset\) used and \(ms_{(6)}^{(6)}\) unused for some \(ms_{(6)}^{(6)}\)

Show:

\[ \left( n_6, (reg_8, ms_7 \cup ms_r \cup \emptyset \cup ms_{(5)}^{(6)}_{\text{unused}}) \right) \in O(W_8) \]

Use Lemma 8. Let \(ms_{(4)}^f\) be given, then

\[ (reg_8, ms_7 \cup ms_r \cup \emptyset \cup ms_{(5)}^{(6)}_{\text{unused}} \cup ms_{(4)}^f) \rightarrow_l (reg_9, ms_7 \cup ms_r \cup \emptyset \cup ms_0 \cup ms_{(4)}^f) \]

where

- \(reg_9(pc) = \text{updatePcPerm}(reg_3(r_0))\) (note \(reg_8(r_0) = reg_3(r_0)\))
- \(reg_9(r_0) = reg_3(r_0)\)
- For all \(r \not\in \{pc, r_0\}, reg_9(r) = 0.\)
\( \text{dom}(m_{s_0}) = \text{dom}(ms_{\text{unused}}^{(5)}) \) and \( \forall a \in \text{dom}(m_{s_0}). m_{s_0}(a) = 0 \)

The execution proceeds as above because \( \iota_x \) in \( W_8 \) is in state 1, so \( ms_7(x) = 1 \) which causes the assertion to succeed. Subsequently the stack and most of the registers are cleared.

Now take \( W_{10} \) to be \( W_9 \) with all the regions in \( \text{dom}([W_3]_{\{\text{temp}\}}) \) reinstated. Now we show the following:

5.3.1. \( W_{10} \models^{\text{pub}} W_3 \)

We have

\[
\forall r \in \text{dom}(W_3). W_3(r) = W_{10}(r)
\]

if the region was permanent in \( W_3 \), then it is there because \( W_{10} \models^{\text{prim}} W_3 \). If it was temporary, then it is there because it was just reinstated. If it was revoked in \( W_3 \), then it is still there because the only reinstated region were the temporary ones in \( W_3 \).

All the future worlds we have been given have been public, so the regions can only have made public transitions. In \( W_3 \) region \( \iota_x \) is in state 0 or 1. In \( W_{10} \) region \( \iota_x \) is in state 1. State 1 can be reached from 0 and 1 using a public transition, so the \( \iota_x \) in \( W_{10} \) is a public future region of the \( \iota_x \) in \( W_3 \).

In other words, all the regions in \( W_3 \) have only taken public transitions compared to the corresponding regions in \( W_{10} \).

The relation between the relevant worlds is sketched out in Figure 4.5.

5.3.2. \( ms_7 \cup ms_r \cup \emptyset \cup m_{s_0} : n_6 - l \) \( W_{10} \)

First notice that from

- \((n_4, \text{reg}_3) \in \mathcal{R}(W_3)\)
- \(ms_3 : n_4 W_3\)
- \(\text{reg}(r_{\text{stk}}).\text{perm} = \text{RWLX}\)

using Lemma 9 we get that there exists a region, \( r_{\text{advstk}} \) such that

\[
W_3(r_{\text{advstk}}) = n^{\text{pub}}_{\text{stk}_a, \text{stk}_b}
\]

and \( \text{dom}(ms_{\text{unused}}) \subseteq [\text{stk}_a, \text{stk}_b] \). Now take \( ms_{\text{advstk}} = ms_r|_{[\text{stk}_a, \text{stk}_b]} \) (notice this not all of \([\text{stk}_a, \text{stk}_b]\) is in the domain of \(ms_r\). We know

\[
ms_7 : n_6 \text{ revokeTemp}(W_8)
\]

and

\[
ms_3 : n_4 W_3
\]

which gives us two partitions say \( P_8 \) and \( P_3 \) respectively. Now define the partition \( P \) as follows:

\[
P(r) = \begin{cases} 
P_8(r) & r \in \text{dom}([W_8]_{\{\text{perm}\}}) \\
ms_{\text{advstk}} \cup m_{s_0} & r = r_{\text{advstk}} \\
P_3(r) & \text{otherwise}
\end{cases}
\]

Now let \( r \in \text{fl}W; n_7 < n_6 - l \), and \( W(r) = (\_ , s_1 , \_ , H) \) and show

\[
(n_7, P(r)) \in H(s)(\xi^{-1}(W_{10})).
\]

Consider the following cases

46
5.3.2.1. \( r \in \text{dom}(\{W_8\}_\text{perm}) \)
Use \ref{10} the fact that \( W_{10} \preceq_{\text{priv}} \text{revokeTemp}(W_8) \) and that permanent regions respect future private world.

5.3.2.2. \( r = r_{\text{advstk}} \)
In this case we know the region is \( n_{\text{advstk}} \), so we need to show

\[
(n_7, ms_{\text{advstk}} \uplus ms_0) \in H_{n_{\text{advstk}}}(1)(\xi^{-1}(W_{10}))
\]

which amounts to showing

\[
\forall a \in \text{dom}(ms_0). (n_7 - 1, ms_0(a)) \in \mathcal{V}(W_{10}),
\]

which is trivial, and

\[
\forall a \in \text{dom}(ms_{\text{advstk}}). (n_7 - 1, ms_{\text{advstk}}(a)) \in \mathcal{V}(W_{10})
\]

here we use that \ref{11} entails

\[
\forall a \in \text{dom}(ms_{\text{advstk}}). (n_4 - 1, ms_{\text{advstk}}(a)) \in \mathcal{V}(W_3)
\]

and the fact that \( \mathcal{V} \) is monotone w.r.t \( \supseteq_{\text{pub}} \), \( W_{10} \supseteq_{\text{pub}} W_3 \), and \( \mathcal{V}(W_{10}) \) is downwards-closed.

5.3.2.3. otherwise
Use \ref{11} \( W_{10} \supseteq_{\text{pub}} W_3 \), and the fact that for a temporary region \( H(s) \) is monotone w.r.t. \( \supseteq_{\text{pub}} \).

5.3.3. \( (n_6 - l, reg_9) \in \mathcal{R}(W_{10}) \)
Most registers are cleared. The only interesting register is \( r_0 \), so show:

\[
(n_6 - l, reg_9(r_0)) \in \mathcal{V}(W_{10})
\]

This follows from \( reg_9(r_0) = reg_3(r_0) \), \( (n_4, reg_3) \in \mathcal{R}(W_3) \), \( \mathcal{V} \) monotone w.r.t \( \supseteq_{\text{pub}} \), \( W_{10} \supseteq_{\text{pub}} W_3 \).

As we were using Lemma \ref{8} we need to show

\[
(n_6 - l, (reg_9, ms_7 \uplus ms_r \uplus \emptyset \uplus ms_0)) \in \mathcal{O}(W_{10})
\]

To this end the use \( reg_3(r_0) = reg_9(r_0) \) and \( (n_4, reg_3(r_0)) \in \mathcal{V}(W_3) \). Assuming that \( reg_9(r_0).\text{perm} \in \{E, RX, RWX, RWLX\} \) (if this is not the case, then it is trivial to show the above as the execution fails), then either the \text{executeCondition} or the \text{enterCondition} hold for appropriate values. Now use that \( n_6 - l < n_4 \) and \( W_{10} \supseteq_{\text{pub}} W_3 \) \ref{5.3.1}

\[
(n_6 - l, \text{updatePcPerm}(reg_9(r_0))) \in \mathcal{E}(W_{10})
\]

now using \ref{5.3.2} and \ref{5.3.3} we get the desired result.

\footnote{We don’t know whether the capability is local or global, but it does not matter as we have a public future world relation between the two worlds.}

\[\square\]

47
5 Logical Relation

5.1 Worlds

Assume a sufficiently large set of states \( \text{State} \) that at least contains the states used in this document.

Definition 3.

\[
\text{Rels} = \{ (\phi_{\text{pub}}, \phi) \in \mathcal{P}(\text{State}^2) \times \mathcal{P}(\text{State}^2) \mid \phi_{\text{pub}}, \phi \text{ is reflexive and transitive and } \phi_{\text{pub}} \subseteq \phi \}
\]

Theorem 1. There exists a c.o.f.e. \( \text{Wor} \) and preorders \( \sqsubseteq_{\text{priv}} \) and \( \sqsubseteq_{\text{pub}} \) such that \((\text{Wor}, \sqsubseteq_{\text{priv}})\) and \((\text{Wor}, \sqsubseteq_{\text{pub}})\) are preordered c.o.f.e.’s and there exists an isomorphism \( \xi \) such that

\[
\xi : \text{Wor} \cong \diamondsuit (\{ \text{revoked} \} + \{ \text{temp} \} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow (\text{Wor} \xrightarrow{\text{mon, ne} \rightarrow \sqsubseteq_{\text{pub}}} \text{UPred(MemSegment)}))) +
\]

\[
\{ \text{perm} \} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow (\text{Wor} \xrightarrow{\text{mon, ne} \rightarrow \sqsubseteq_{\text{priv}}} \text{UPred(MemSegment)})))
\]

and for \( W, W' \in \text{Wor} \)

\[
W' \sqsubseteq_{\text{priv}} W \Leftrightarrow \xi(W') \sqsubseteq_{\text{priv}} \xi(W)
\]

and

\[
W' \sqsubseteq_{\text{pub}} W \Leftrightarrow \xi(W') \sqsubseteq_{\text{pub}} \xi(W)
\]

We now define the regions to be

\[
\text{Region} = \{ \text{revoked} \} \cup
\]

\[
\{ \text{temp} \} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow (\text{Wor} \xrightarrow{\text{mon, ne} \rightarrow \sqsubseteq_{\text{pub}}} \text{UPred(MemSegment)}))) \cup
\]

\[
\{ \text{perm} \} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow (\text{Wor} \xrightarrow{\text{mon, ne} \rightarrow \sqsubseteq_{\text{priv}}} \text{UPred(MemSegment)})))
\]

Let \( \iota.v \) be the projection of the view of a region.

And the worlds are

\[
\text{World} = \text{RegionName} \xrightarrow{\delta_R} \text{Region}
\]

where \( \text{RegionName} = \mathbb{N} \).
The two private future region relations satisfies the following properties:

\[(s, s') \in \phi \quad (v, \phi_{pub}, \phi, H) = (v', \phi'_{pub}, \phi', H')\]

\[r \in \text{Region} \quad r \preceq_{\text{prv}} \text{revoked}\]

The two public future region relations satisfies the following properties:

\[(s, s') \in \phi_{pub} \quad (v, \phi_{pub}, \phi, H) = (v', \phi'_{pub}, \phi', H')\]

\[(\text{temp, } s, \phi_{pub}, \phi, H) \preceq_{\text{pub}} \text{revoked}\]

The two future world relations satisfy the following properties: They allow for any extension of the current world and all existing worlds are allowed to move to an appropriate future region. That is

\[\text{dom}(W) \supseteq \text{dom}(W') \quad \forall r \in \text{dom}(W). W'(r) \preceq_{\text{pub}} W(r)\]

\[\text{dom}(W) \supseteq \text{dom}(W') \quad \forall r \in \text{dom}(W). W'(r) \preceq_{\text{prv}} W(r)\]

Proof of Theorem 1. The theorem follows from a more general solution theorem for the category of preordered c.o.f.e.'s, see Birkedal et al. [2010], Birkedal and Bizjak [2014] and Bizjak [2017]. We define two functors \(F_1\) and \(F_2\) from \(P^{op} \times P^{op}\) to \(P\).

\[F_1((X, \preceq_{\text{prv}}'), (Y, \preceq_{\text{pub}}')) =\]

\[\left\langle \begin{array}{c}
\uparrow (\mathbb{N} \xrightarrow{\delta_{\text{fin}}} (\{\text{revoked}\} + \\
\{\text{temp}\} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow (Y, \preceq_{\text{pub}}') \xrightarrow{\text{mon, ne}} \text{UPred(MemSegment)})) + \\
\{\text{perm}\} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow ((X, \preceq_{\text{prv}}') \xrightarrow{\text{mon, ne}} \text{UPred(MemSegment)})))\right)\right\rangle, \preceq_{\text{prv}}\]

and

\[F_2((X, \preceq_{\text{prv}}'), (Y, \preceq_{\text{pub}}')) =\]

\[\left\langle \begin{array}{c}
\uparrow (\mathbb{N} \xrightarrow{\delta_{\text{fin}}} (\{\text{revoked}\} + \\
\{\text{temp}\} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow ((Y, \preceq_{\text{pub}}') \xrightarrow{\text{mon, ne}} \text{UPred(MemSegment)})) + \\
\{\text{perm}\} \times \text{State} \times \text{Rels} \times (\text{State} \rightarrow ((X, \preceq_{\text{prv}}') \xrightarrow{\text{mon, ne}} \text{UPred(MemSegment)})))\right)\right\rangle, \preceq_{\text{pub}}\]

The orderings \(\succeq_{\text{prv}}\) and \(\succeq_{\text{pub}}\) used in the definition of \(F_1\) and \(F_2\) are defined by the properties given above. Note that the image of \(F_1\) and \(F_2\) only differ in the ordering relation, i.e., letting \(U\) denote the forgetful functor from the category of preordered c.o.f.e.'s to the category of c.o.f.e.'s, we have \(U \circ F_1 = U \circ F_2\). From Bizjak [2017] it then follows that there exists a c.o.f.e. Wor and two preorderings \(\succeq_{\text{prv}}\) and \(\succeq_{\text{pub}}\) and an isomorphism \(\xi\) satisfying the properties claimed in theorem. (Here, in the proof, we have written the ordering explicitly on the c.o.f.e. when using monotone non-expansive functions; in the theorem formulation we have instead annotated the arrow to indicate which ordering is used.)

Erase all but a set of views:

\[ [W]_S \triangleq \lambda r. \begin{cases} W(r) & W(r).v \in S \\ \bot & \text{otherwise} \end{cases} \]

Define the function \( \text{active}(\cdot) \) as follows:

\[
\text{active} : \text{World} \to 2^{\text{RegionName}} \\
\text{active}(W) \triangleq \text{dom}([W]_{\{\text{perm, temp}\}})
\]

Memory segment satisfaction:

\[
\text{ms} :_n W \text{ iff } \left\{ \begin{array}{l}
\exists P : \text{active}(W) \to \text{MemSegment}, \\
\text{ms} :_{n,P} W
\end{array} \right.
\]

\[
\text{ms} :_{n,P} W \text{ iff } \left\{ \begin{array}{l}
\text{ms} = \biguplus_{r \in \text{active}(W)} P(r) \land \\
\forall r \in \text{active}(W), \\
\exists H, s, \\
W(r) = (\_s, \_s, \_H) \land \\
(n, P(r)) \in H(s)(\xi^{-1}(W))
\end{array} \right.
\]

Standard regions for when writing locally is permitted:

\[
\iota_{\text{pwl}} : \mathcal{P} \to \text{Region} \\
\iota_{\text{pwl}} A \triangleq (\text{temp}, 1, =, =, H_{\text{pwl}} A)
\]

\[
H_{\text{pwl}} : \mathcal{P}(\text{Addr}) \to \text{State} \to (\text{World} \upharpoonright_{\text{up}} \text{UPred}(\text{MemSegment}))
\]

\[
H_{\text{pwl}} A s W \triangleq \left\{ (n, ms) \mid \begin{array}{l}
\text{dom}(ms) = A \land \\
\forall a \in A. (n - 1, ms(a)) \in V(\xi(W))
\end{array} \right\} \cup \{0, ms\}
\]

Revoking all temporary regions:

\[
\text{revokeTemp} : \text{World} \to \text{World} \\
\text{revokeTemp}(W) \triangleq \lambda r. \begin{cases} \text{revoked} & \text{if } W(r) = (\text{temp}, s, \phi_{\text{pub}}, \phi, H) \\
W(r) & \text{otherwise} \end{cases}
\]

Further define

\[
\iota_{\text{pwl}}_{\text{base}, \text{end}} \triangleq \iota_{\text{pwl}}([\text{base, end}])
\]
Standard regions for when write local is not allowed:

\[ \iota^{\text{nwlt}} : \mathcal{P}(\text{Addr}) \rightarrow \text{Region} \]
\[ \iota^{\text{nwlt}} A \overset{\text{def}}{=} (\text{temp}, 1, =, =, H^{\text{nwlt}} A) \]

\[ \iota^{\text{nwlt}, p} : \mathcal{P}(\text{Addr}) \rightarrow \text{Region} \]
\[ \iota^{\text{nwlt}, p} A \overset{\text{def}}{=} (\text{perm}, 1, =, =, H^{\text{nwlt}} A) \]

\[ H^{\text{nwlt}} : \mathcal{P}(\text{Addr}) \rightarrow \text{State} \rightarrow (\text{Wor} \underset{\text{perm}}{\overset{\text{non-local}}{\rightarrow}} \text{UPred(MemSegment)}) \]

\[ H^{\text{nwlt}} A s \hat{W} \overset{\text{def}}{=} \left\{ \begin{array}{ll} \{ \text{dom}(ms) = A \land \\
\forall a \in A. \ 	ext{ms}(a) \text{ is non-local} \land \ \\
(n - 1, \text{ms}(a)) \in \mathcal{V}(\xi(\hat{W})) \} & \cup \{(0, ms)\} \end{array} \right. \]

Further define

\[ \iota^{\text{nwlt}, \text{end}, \text{base}} \overset{\text{def}}{=} \iota^{\text{nwlt}}([\text{base}, \text{end}]) \]
\[ \iota^{\text{nwlt}, p, \text{end}, \text{base}} \overset{\text{def}}{=} \iota^{\text{nwlt}, p}([\text{base}, \text{end}]) \]

For convenience define

\[ \text{localityReg}(g, W) \overset{\text{def}}{=} \begin{cases} \text{dom}([W]_{\text{perm}, \text{temp}}) & \text{if } g = \text{LOCAL} \\
\text{dom}([W]_{\text{perm}}) & \text{if } g = \text{GLOBAL} \end{cases} \]

localityReg(LOCAL, W) are the regions that local capabilities may govern - that is permanent and temporary regions. localityReg(GLOBAL, W) are the regions that global capabilities may govern - that is permanent regions. Now define the following function

We need a notion of subset between regions that is almost n-subset, but not quite. The only difference is that the view part of a region is disregarded. Define “semi n-subset” and “semi n-supset” as:

\[ (s, \phi_{\text{pub}}, \phi) = (s', \phi'_{\text{pub}}, \phi') \quad \forall \hat{W}, H s W \overset{n}{\subseteq} H' s' \hat{W} \]
\[ (v, s, \phi_{\text{pub}}, \phi, H) \overset{n}{\subseteq} (v', s', \phi'_{\text{pub}}, \phi', H') \]

5.2 The logical relation

The logical relation is defined by several mutual recursive definitions. In order to handle this mutual recursion and show that this definitions are well-defined, Banach’s fixed-point theorem can be used. We have omitted the details of this construction here, but it is done by parameterising all the definitions by the value relation.
\( \tau = (v, s, \phi_{pub}, \phi, H) \) is address-stratified iff

\[ \forall s', W, n, ms, ms'. \quad (n, ms), (n, ms') \in H \quad s' \quad W \Rightarrow \quad \text{dom}(ms) = \text{dom}(ms') \wedge \forall a \in \text{dom}(ms). (n, ms[a \mapsto ms'(a)]) \in H \quad s' \quad W \]

| writeCondition : \(((\text{Addr} \times \text{Addr}) \rightarrow \text{Region}) \times \text{Global}) \rightarrow \text{World} \xrightarrow{\text{mon.} \neq} \text{UPred}(\text{Addr}^2) |
| writeCondition(\iota, g)(W) = |
| \{(n, (\text{base}, \text{end})) | \exists r \in \text{localityReg}(g, W). \quad \exists [\text{base}', \text{end}'] \supseteq [\text{base}, \text{end}]. \quad W(r) \xrightarrow{n-1} \iota_{\text{base}', \text{end}'} \text{ and } \quad W(r) \text{ is address-stratified} \} |

| readCondition : \text{Global} \rightarrow \text{World} \xrightarrow{\text{mon.} \neq} \text{UPred}(\text{Addr}^2) |
| readCondition(g)(W) = |
| \{(n, (\text{base}, \text{end})) | \exists r \in \text{localityReg}(g, W). \quad \exists [\text{base}', \text{end}'] \supseteq [\text{base}, \text{end}]. \quad W(r) \xrightarrow{n} \iota_{\text{base}', \text{end}'} \} |

| executeCondition(g)(W) = |
| \{(n, (\text{perm}, \text{base}, \text{end})) | \forall n' < n. \quad \forall W' \supseteq W. \quad \forall a \in [\text{base}', \text{end}'] \subseteq [\text{base}, \text{end}]. \quad (n', ((\text{perm}, g), \text{base}', \text{end}', a)) \in \mathcal{E}(W') \} |

| enterCondition(g)(W) = |
| \{(n, (\text{base}, \text{end}, a)) | \forall n' < n. \quad \forall W' \supseteq W. \quad (n', ((\text{RX}, g), \text{base}, \text{end}, a)) \in \mathcal{E}(W') \} |

where \( g = \text{LOCAL} \Rightarrow \exists = \mathcal{E}_{\text{pub}} \) and \( g = \text{GLOBAL} \Rightarrow \exists = \mathcal{E}_{\text{priv}} \)
Now define the value relation as follows:

\[ \mathcal{V} : \text{World} \xrightarrow{\text{ms}, \text{ms}_f} \text{UPred(Word)} \]

\[ \mathcal{V} \overset{def}{=} \lambda W. \{ (n, i) \mid i \in \mathbb{Z} \cup \{ \infty \} \} \cup \]
\[ \{ (n, ((\text{O}, g), \text{base}, \text{end}, a)) \} \cup \]
\[ \{ (n, ((\text{RO}, g), \text{base}, \text{end}, a)) \} \cup \]
\[ (n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W) \} \cup \]
\[ \{ (n, ((\text{RW}, g), \text{base}, \text{end}, a)) \} \cup \]
\[ (n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W) \} \]
\[ \{ (n, ((\text{RWL}, g), \text{base}, \text{end}, a)) \} \cup \]
\[ (n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W) \} \cup \]
\[ \{ (n, ((\text{RX}, g), \text{base}, \text{end}, a)) \} \cup \]
\[ (n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W) \} \cup \]
\[ \{ (n, ((\text{RX}, \text{end}), \text{base}, \text{end}, a)) \} \cup \]
\[ (n, (\text{base}, \text{end})) \in \text{execCondition}(g)(W) \} \}

\[ \mathcal{O} : \text{World} \xrightarrow{\text{ms}, \text{ms}_f} \text{UPred}(\text{Reg} \times \text{MemSegment}) \]

\[ \mathcal{O} \overset{def}{=} \lambda W. \{ (n, (\text{reg}, \text{ms})) \mid \forall \text{ms}_f, \text{mem}', i \leq n. \]
\[ (\text{reg}, \text{ms} \oplus \text{ms}_f) \rightarrow_i (\text{halted}, \text{mem}') \]
\[ \Rightarrow \exists W' \overset{\text{priv}}{=} W. \exists \text{ms}_r, \text{ms}' . \]
\[ \text{mem}' = \text{ms}' \oplus \text{ms}_r \oplus \text{ms}_f \wedge \]
\[ \text{ms}'_{n-i} W' \}

53
\[ \mathcal{R} : \text{World} \xrightarrow{\text{mon}, \to} \text{UPred(Reg)} \]
\[ \mathcal{R} \overset{\text{def}}{=} \lambda W. \{(n, \text{reg}) | \forall r \in \text{RegisterName} \setminus \{\text{pc}\}. (n, \text{reg}(r)) \in \mathcal{V}(W)\} \]

\[ \mathcal{E} : \text{World} \xrightarrow{\text{w}} \text{UPred(Word)} \]
\[ \mathcal{E} \overset{\text{def}}{=} \lambda W. \{(n, \text{pc}) | \forall n' \leq n. \forall (n', \text{reg}) \in \mathcal{R}(W). \forall ms :n' W. (n', \text{reg}[\text{pc} \mapsto \text{pc}], ms) \in \mathcal{O}(W)\} \]

### 5.3 Useful regions

Static region used for parts of memory that should not change.

\[ \iota_{\text{sta}}(v, ms) = (v, 1, =, =, H_{\text{sta}} ms) \]
\[ H_{\text{sta}} ms s W = \{(n, ms) | n > 0\} \cup \{(0, ms') | ms' \in \text{Mem}\} \]

Static region used for parts of memory that should not change and where you pass control to untrusted code.

\[ \iota_{\text{sta},u}(v, ms) = (v, 1, =, =, H_{\text{sta},u} ms) \]
\[ H_{\text{sta},u} ms s W = \left\{ (n, ms') | ms' = ms \land \forall a \in \text{dom}(ms). ms(a) \text{ is non-local} \land (n - 1, ms(a)) \in \mathcal{V}(\xi(W)) \right\} \cup \{(0, ms') | ms' \in \text{Mem}\} \]

\[ \iota_{\text{cnst}}(v, n) = (v, 1, =, =, H_{\text{cnst}} n) \]
\[ H_{\text{cnst}} n' s W = \{(n, ms) | n > 0 \land \forall a \in \text{dom}(ms). ms(a) = n'\} \cup \{(0, ms') | ms' \in \text{Mem}\} \]

### 5.4 Lemmas

#### 5.4.1 Anti-reduction for the observation relation

**Lemma 7** (Failing terms are in \( \mathcal{O} \) and \( \mathcal{E} \)). If \( \text{reg}, ms \uplus ms_f \to^* \text{ failed for all } ms_f \), then \( (n, (\text{reg}, ms)) \in \mathcal{O}(W) \) for any \( W \).

If \( \text{reg}[\text{pc} \mapsto w], ms \to^* \text{ failed for all } \text{reg}, ms \), then \( (n, w) \in \mathcal{E}(W) \) for any \( W \). □

**Proof.** Follows from the definitions of \( \mathcal{O}(W) \) and \( \mathcal{E}(W) \) using an (omitted) determinacy result. □
Lemma 8 (Anti-reduction for $O$).

$$\forall n, n', i, \text{reg}, \text{reg}', ms, ms', ms_r, W, W'.
\quad n' \geq n - i \land W' \supseteq \text{priv} W \land
\quad (\forall ms_f, (\text{reg}, ms \uplus ms_r \uplus ms_f) \rightarrow \text{reg}', ms' \uplus ms_r \uplus ms_f) \land
\quad (n', (\text{reg}', ms')) \in O(W')
\quad \Rightarrow (n, (\text{reg}, ms \uplus ms_r)) \in O(W)$$

Proof of Lemma 8. Assume

1. $n' \geq n - i$
2. $W_2 \supseteq \text{priv} W_1$
3. $\forall ms_f, (\text{reg}, ms \uplus ms_r \uplus ms_f) \rightarrow (\text{reg}', ms' \uplus ms_r \uplus ms_f)$
4. $(n', (\text{reg}', ms')) \in O(W_2)$

Show $(n, (\text{reg}, ms \uplus ms_r)) \in O(W_1)$

To this end let $ms_{frame}$, $m'$ and $j$ be given and assume

$$(\text{reg}, ms \uplus ms_r \uplus ms_{frame}) \rightarrow j (\text{halted}, m') \quad (12)$$

From 3. instantiated with $ms_{frame}$ we know

$$(\text{reg}, ms \uplus ms_r \uplus ms_{frame}) \rightarrow_j (\text{reg}', ms' \uplus ms_r \uplus ms_{frame}) \quad (13)$$

Using 12 and 13, we get

$$(\text{reg}', ms' \uplus ms_r \uplus ms_{frame}) \rightarrow_{j-i} (\text{halted}, m')$$

Using this with 4. and $ms_r \uplus ms_{frame}$ as frame, we get $W_3 \supseteq \text{priv} W_2$, $ms''$ and $ms_{rev}$ such that

5. $m' = ms'' \uplus ms_{rev} \uplus (ms_r \uplus ms_{frame})$
6. $ms'' :_{n'-(j-i)} W_3$

Now use $ms_r \uplus ms_{rev}$ as the “revoked” memory, $ms''$ as the memory that satisfies some invariants, and $W_3$ as the desired world, then 5. gives us the split and by downwards closure 6. gives us the desired memory satisfaction.

5.4.2 Standard regions

Lemma 9. For all $W$, base, end, $n$, $ms$ if

- $ms :_{n} W$
- $(n, ((\text{perm}, g), \text{base}, \text{end}, a)) \in V(W)$
- $\text{base} \leq \text{end}$

55
\* \( \text{perm} \in \{ \text{rwLx}, \text{rwX} \} \)

then

\[
\exists r, \text{base'}, \text{end'}. [\text{base}, \text{end}] \subseteq [\text{base'}, \text{end'}] \land W(r) \models t_{\text{base'}, \text{end'}}^\text{pwL}
\]

**Proof of Lemma 9.** Assume

1. \((n, ((\text{rwLx}, g), b, e, a)) \in \mathcal{V}(W)\)
2. \(ms :_n W\)

From Assumption 1., we get \(r_1, r_2, b_1, b_2, e_1, e_2\) such that

3. \(r_1 \in \text{localityReg}(g, W)\)
4. \(r_2 \in \text{localityReg}(g, W)\)
5. \([b, e] \subseteq [b_1, e_1]\)
6. \([b, e] \subseteq [b_2, e_2]\)
7. \(W(r_1) \models \text{pwl}_{b_1, e_1}\)
8. \(W(r_2) \models \text{pwl}_{b_2, e_2}\)
9. \(W(r_2)\) is address-stratified.

From Assumption 2., we get \(p\) s.t.

\(ms :_n W\)

Say \(P(r_1) = ms_1\) and \(P(r_2) = ms_2\). First from \((n, ms_1) \in W(r_1).H W(r_1).s \xi^{-1}(W)\) using , we get \((n, ms_1) \in H^{\text{pwl}}_{b_1, e_1} 1 \xi^{-1}(W)\) which means \(\text{dom}(ms_1) = [b_1, e_1]\).

Second we know \((n, [b_2 \mapsto 0, \ldots, e_2 \mapsto 0]) \in H^{\text{pwl}}_{b_2, e_2} 1 \xi^{-1}(W)\) and \((n, ms_2) \in W(r_2).H W(r_2).s \xi^{-1}(W)\) which by Assumption 8. and 9. means \(\text{dom}(ms_2) = [b_2, e_2]\).

Now assume for contradiction \(r_1 \neq r_2\), then we have a contradiction with \(ms :_n W\) because \(ms_1\) and \(ms_2\) are not disjoint (by Assumptions 5. and 6.). So \(r_1 = r_2\) which also means \([b_1, e_1] = [b_2, e_2]\), so from Assumption 5. and 8., we get \(W(r_1) \models \text{pwl}_{b_1, e_1}\) which by Lemma 24 means \(W(r_1) \models \text{pwl}_{b_1, e_1}\).

**Lemma 10.** \(H^{\text{pwl}}_{\text{base}, \text{end}} s\) is monotone w.r.t \(\preceq\text{pub}\) for all \(s \in \text{State}\) and \(\text{base}\) and \(\text{end}\)

**Proof of Lemma 10.** Let \(\hat{W}' \preceq\text{pub} \hat{W}\) be given and let

\[
(n, ms) \in H^{\text{pwl}}_{\text{base}, \text{end}} s \hat{W}
\]

and show

\[
(n, ms) \in H^{\text{pwl}}_{\text{base}, \text{end}} s \hat{W}'
\]

From 14 we get \(\text{dom}(ms) = [\text{base}, \text{end}]\). Now let \(a \in [\text{base}, \text{end}]\) be given and show

\[
(n - 1, ms(a)) \in \mathcal{V}(\xi(\hat{W}'))
\]

now this follows from Lemma 77 \(\hat{W}' \preceq\text{pub} \hat{W}\), Theorem 1 and Assumption 14.
Lemma 11. \( \text{pwl}_{\text{base, end}} \) is a region for all base and end.

Proof of Lemma 11. Follows from Lemma 10.

Lemma 12. \( \text{pwl}_{\text{base, end}} \) is address-stratified.

Proof. Easy unfolding of definitions.

Lemma 13. \( H_{\text{nwl, base, end}} \) is monotone w.r.t \( \preceq_{\text{priv}} \) for all \( s \in \text{State} \) and base and end.

Proof of Lemma 13. Let \( \hat{W}' \preceq_{\text{priv}} \hat{W} \) be given and let
\[
(n, ms) \in H_{\text{nwl, base, end}} s \hat{W} \tag{15}
\]
and show
\[
(n, ms) \in H_{\text{nwl, base, end}} s \hat{W}'
\]
From 15. we get \( \text{dom}(ms) = [\text{base, end}] \). Now let \( a \in [\text{base, end}] \) be given and show
1. \( ms(a) \) is non-local
2. \((n - 1, ms(a)) \in V(\xi(\hat{W}'))\)

Lemma 14. \( \text{nwl}_{\text{base, end}} \) is a region for all base and end.


Lemma 15. \( \text{nwl}_{\text{base, end}} \) is address-stratified.

Proof. Easy unfolding of definitions.

Lemma 16. \( \text{nwl, p}_{\text{base, end}} \) is a region for all base and end.


Lemma 17. \( \text{sta}(v, ms) \) is a region for all \( v \in \{\text{perm, temp}\} \) and ms.

Proof of Lemma 17. \( H_{\text{sta}} \) does not depend on \( \hat{W} \), so it is trivial to show the necessary non-expansive and monotonicity requirements.

Lemma 18. \( H_{\text{sta, u}}(ms) \) is monotone w.r.t \( \preceq_{\text{priv}} \) for all \( s \in \text{State} \) and ms.

Proof of Lemma 18. Let \( \hat{W}' \preceq_{\text{priv}} \hat{W} \) be given and let
\[
(n, ms') \in H_{\text{sta, u}}(ms) s \hat{W} \tag{16}
\]
and show
\[
(n, ms') \in H_{\text{sta, u}}(ms) s \hat{W}'
\]
From 16. we get \( ms' = ms \). Now let \( a \in \text{dom}(ms) \) be given and show
1. \( ms(a) \) is non-local
2. \((n - 1, ms(a)) \in V(\xi(\hat{W}'))\)
follows trivially from Assumption (which we just argued), $\hat{W} \supseteq_{\text{priv}} W$, Theorem 1 and Lemma 80.

**Lemma 19.** $\iota_{\text{sta},u}(v, ms)$ is a region for all $v \in \{\text{perm}, \text{temp}\}$ and $ms$.

*Proof of Lemma 19.* Follows from Lemma 18 and Lemma 71.

**Lemma 20.**

$$H_{\text{nwl base}, \text{end}}^n s \hat{W} \subseteq H_{\text{pwl base}, \text{end}}^n s \hat{W}$$

*Proof of Lemma 20.* Trivial. Let

$$(n, ms) \in H_{\text{nwl base}, \text{end}}^n s \hat{W}$$

and show

$$(n, ms) \in H_{\text{pwl base}, \text{end}}^n s \hat{W}$$

From the assumption, we get $\text{dom}(ms) = [\text{base}, \text{end}]$. We further need to show

$$\forall a \in \text{dom}(ms). (n - 1, ms(a)) \in \mathcal{V}(\hat{W})$$

Given $a$, we know from the assumption that

$$(n - 1, ms(a)) \in \mathcal{V}(\hat{W})$$

**Lemma 21.**

$$\forall n \in \mathbb{N}. \forall \text{base, end} \in \text{Addr.}$$

$$\iota_{\text{nwl}, \text{base}, \text{end}}^n \subseteq \iota_{\text{pwl}, \text{base}, \text{end}}^n$$

*Proof of Lemma 21.* Let $n$, base, end be given and show

$$\iota_{\text{nwl}, \text{base}, \text{end}}^n \subseteq \iota_{\text{pwl}, \text{base}, \text{end}}^n$$

They agree on the state and transition systems, so given $\hat{W}$ it suffices to show

$$H_{\text{nwl base}, \text{end}}^n \hat{W} \subseteq H_{\text{pwl base}, \text{end}}^n \hat{W}$$

which is true by Lemma 20.

**Lemma 22.**

$$\forall n \in \mathbb{N}. \forall \text{base, end} \in \text{Addr.}$$

$$\iota_{\text{nwl}, \text{base}, \text{end}}^n \subseteq \iota_{\text{pwl}, \text{base}, \text{end}}^n$$

*Proof of Lemma 22.* Follows from Lemma 20 (see proof of Lemma 21).
Lemma 23.

\[ \forall n \in \mathbb{N}. \forall base, end \in \text{Addr}. \forall v \in \{\text{perm, temp}\}. \]

\[ \text{dom}(ms) = [base, end] \Rightarrow \]

\[ _{\text{sta}, u}^{n} \iota_{\text{base, end}}(v, ms) \supseteq _{\text{pwl}}^{n} \iota_{\text{base, end}} \]

Proof of Lemma 23. Essentially the same as the proof of Lemma 21 and Lemma 20.

Lemma 24.

\[ \forall n \in \mathbb{N}. \forall base, end, b \in \text{Addr}. \forall \iota \in \text{Region} \]

\[ \iota \frac{n}{pwl} \iota_{\text{base, end}} \land base \leq end \Rightarrow \iota \frac{n}{pwl} \iota_{\text{base, end}} \]

Proof of Lemma 24. For \( n = 0 \) it is trivial, so assume \( n > 0 \). Say \( \iota = (v, s, \phi_{\text{pub}}, \phi, H) \), then by \( \frac{n}{\sim} \) we know \( s = 1, \phi_{\text{pub}} \equiv \phi \equiv =, \) and \( H = H_{\text{base, end}}^{\text{pwl}} \). It remains to show that \( v = \text{temp} \). To do so, we show that it cannot be the case that \( v = \text{perm} \). If \( v = \text{perm} \), then \( H \) must be monotone with respect to \( \sqsupseteq_{\text{priv}} \). If we can show that this is not the case, then for \( \iota \) to be a region it must be the case that \( v \neq \text{perm} \) and thus \( v = \text{temp} \).

To this end let \( b \notin [base, end] \) and define the worlds:

\[ \xi(W) = [0 \mapsto _{\text{pwl}}^{n} \iota_{\text{base, end}}] \]

\[ [1 \mapsto _{b,b}^{l}] \]

\[ \xi(W') = [0 \mapsto _{\text{pwl}}^{n} \iota_{\text{base, end}}] \]

\[ [1 \mapsto \text{revoked}] \]

For these two worlds, we have \( \xi(W') \sqsupseteq_{\text{priv}} \xi(W) \) and from mono. of \( \xi^{-1} \), we have \( W' \sqsupseteq \sqsupseteq_{\text{priv}} W \).

Now define the following memory segment:

\[ ms = [base \mapsto ((\text{RO, LOCAL}), b, b, b), base + 1 \mapsto 0, \ldots, end \mapsto 0] \]

It is the case that

\[ (n, ms) \in H \ 1 \ W \]

but

\[ (n, ms) \notin H \ 1 \ W' \]

as it is not the case that

\[ (n - 1, ((\text{RO, LOCAL}), b, b, b)) \in \forall(\xi(W')). \]

The only other option that remains is \( v = \text{temp} \).

5.4.3 Observation relation

Lemma 25 (Observation relation (O) non-expansive).

\[ W \triangleq W' \Rightarrow O(W) \triangleq O(W') \]

Proof of Lemma 25.
5.4.4 Register-file relation

Lemma 26 (Register-file relation \((R)\) non-expansive).

\[ W \sqsubseteq W' \Rightarrow R(W) \sqsubseteq R(W') \]

Proof of Lemma 26.

Lemma 27 (Register-file relation \((R)\) monotone wrt \(\sqsupseteq_{pub}\)).

\[ W' \sqsupseteq_{pub} W \Rightarrow R(W') \sqsupseteq_{pub} R(W) \]

Proof of Lemma 27.

5.4.5 Expression relation

Lemma 28 (Expression relation \((E)\) non-expansive).

\[ W \sqsubseteq W' \Rightarrow E(W) \sqsubseteq E(W') \]

Proof of Lemma 28.

5.4.6 Permission based conditions

Lemma 29. If \((n, (\text{base}, \text{end})) \in \text{readCondition}(g)(\text{revokeTemp}(W))\) then \((n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W)\)

Proof of Lemma 29.

\(n, (\text{base}, \text{end})) \in \text{readCondition}(g)(\text{revokeTemp}(W))\)

Gives \(r \in \text{localityReg}(g, \text{revokeTemp}(W))\) such that

\[ \forall [\text{base}', \text{end}'] \subseteq [\text{base}, \text{end}]. \text{revokeTemp}(W)(r) \sqsubseteq_{\text{pub}} t_{[\text{base}', \text{end}']}^{\text{pwl}} \]

Notice \(\text{revokeTemp}(W)(r)\) is a perm region, so \(\text{revokeTemp}(W)(r) = W(r)\). Using \(r\) as witness, the result is immediate.

Lemma 30. If \((n, (\text{base}, \text{end})) \in \text{writeCondition}(\iota, g)(\text{revokeTemp}(W))\) then \((n, (\text{base}, \text{end})) \in \text{writeCondition}(\iota, g)(W)\)
Proof of Lemma 30.

\[(n, (\text{base, end})) \in \text{writeCondition}(\iota, g)(\text{revokeTemp}(W))\]

Gives \(r \in \text{localityReg}(g, \text{revokeTemp}(W))\) such that

\[\forall [\text{base}', \text{end}'] \subseteq [\text{base, end}] . \text{revokeTemp}(W)(r) \overset{n-1}{\not\succcurlyeq} \iota[\text{base}', \text{end}']\]

and

\[\text{revokeTemp}(W)(r)\] is address-stratified

Notice \(\text{revokeTemp}(W)(r)\) is a perm region, so \(\text{revokeTemp}(W)(r) = W(r)\). Using \(r\) as witness, the result is immediate.

Lemma 31. If

\[- (n, (\text{perm, base, end})) \in \text{executeCondition}(g)(\text{revokeTemp}(W))\]

then

\[(n, (\text{perm, base, end})) \in \text{executeCondition}(g)(W)\]

Proof of Lemma 31. Use Lemma 69.

Lemma 32. If

\[- (n, (a, base, end)) \in \text{executeCondition}(g)(\text{revokeTemp}(W))\]

then

\[(n, (a, base, end)) \in \text{executeCondition}(g)(W)\]

Proof of Lemma 32. Use Lemma 69.

Lemma 33. If

\[(n, (\text{base, end})) \in \text{writeCondition}(\iota^{\text{pwl}}, \text{local})(W)\]

then

\[(n, (\text{base, end})) \in \text{writeCondition}(\iota^{\text{nwl}}, \text{local})(W)\]

Proof of Lemma 33. Follows from Lemma 22.

Lemma 34 (\text{readCondition} monotone w.r.t \(\not\succcurlyeq^{\text{pub}}\)). If

\[- W' \not\succcurlyeq^{\text{pub}} W\]

\[- (n, (\text{base, end})) \in \text{readCondition}(g)(W)\]

then

\[(n, (\text{base, end})) \in \text{readCondition}(g)(W')\]

Proof of Lemma 34.
Lemma 35 (readCondition global monotonicity w.r.t $\sqsupseteq^{\text{priv}}$). If

- $W' \sqsupseteq^{\text{priv}} W$
- $(n, (\text{base}, \text{end})) \in \text{readCondition}(\text{GLOBAL})(W)$

then

- $(n, (\text{base}, \text{end})) \in \text{readCondition}(\text{GLOBAL})(W')$

Proof of Lemma 35. readCondition(\text{GLOBAL})(W) picks a perm region from $W$. perm regions are persistent over $\sqsupseteq^{\text{priv}}$, so we can use the region that the assumption gives us.

Lemma 36 (readCondition downwards-closed). If

- $n' \leq n$
- $(n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W)$

then

- $(n', (\text{base}, \text{end})) \in \text{readCondition}(g)(W')$

Proof of Lemma 36.

Lemma 37 (writeCondition monotone w.r.t $\sqsupseteq^{\text{pub}}$). If

- $W' \sqsupseteq^{\text{pub}} W$
- $\iota \in \{\iota_{\text{pwl}}, \iota_{\text{nwl}}, \iota_{\text{nwl},p}\}$
- $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\iota, g)(W)$

then

- $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\iota, g)(W')$

Proof of Lemma 37.

Lemma 38 (writeCondition global monotonicity w.r.t $\sqsupseteq^{\text{priv}}$). If

- $W' \sqsupseteq^{\text{priv}} W$
- $\iota \in \{\iota_{\text{nwl}}, \iota_{\text{nwl},p}\}$
- $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\iota, \text{GLOBAL})(W)$

then

- $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\iota, \text{GLOBAL})(W')$

Proof of Lemma 38. writeCondition(\iota, \text{GLOBAL})(W) picks a perm region from $W$. perm regions are persistent over $\sqsupseteq^{\text{priv}}$, so we can use the region that the assumption gives us.

Lemma 39 (writeCondition downwards-closed). If
• \( n' \leq n \)
• \( \iota \in \{ \iota_{pwl}, \iota_{nwl}, \iota_{(nwl,p)} \} \)
• \( (n, (\text{base, end})) \in \text{writeCondition}(\iota, g)(W) \)

then

\[ (n', (\text{base, end})) \in \text{writeCondition}(\iota, g)(W) \]

Proof of Lemma 39.

Lemma 40 (\text{execCondition} monotone w.r.t \( \succeq^{pub} \)). If

• \( W' \succeq^{pub} W \)
• \( \text{perm} \in \{ \text{RX, RWX, RWLX} \} \)
• \( (n, (\text{perm, base, end})) \in \text{executeCondition}(g)(W) \)

then

\[ (n, (\text{perm, base, end})) \in \text{executeCondition}(\iota, g)(W') \]

Proof of Lemma 40.

Lemma 41 (\text{execCondition} global monotonicity w.r.t \( \succeq^{priv} \)). If

• \( W' \succeq^{priv} W \)
• \( \text{perm} \in \{ \text{RX, RWX} \} \)
• \( (n, (\text{perm, base, end})) \in \text{executeCondition}(\text{GLOBAL})(W) \)

then

\[ (n, (\text{perm, base, end})) \in \text{executeCondition}(\text{GLOBAL})(W') \]

Proof of Lemma 41. Assume \( W_2 \succeq^{priv} W_1 \), \( \text{perm} \in \{ \text{RX, RWX} \} \) and \( (n, (\text{perm, base, end})) \in \text{executeCondition}(\text{GLOBAL})(W_1) \). Now let \( W_3 \succeq^{priv} W_2 \), \( a \in [\text{base}', \text{end}'] \subseteq [\text{base, end}] \), and \( n' < n \), and show

\[ (n, ((\text{perm, GLOBAL}), \text{base}', \text{end}', a)) \in \mathcal{E}(W_3) \]

by transitivity we have \( W_3 \succeq^{priv} W_1 \), so the result follows from \( (n, (\text{perm, base, end})) \in \text{executeCondition}(\text{GLOBAL})(W_1) \).

Lemma 42 (\text{execCondition} downwards-closed). If

• \( n' \leq n \)
• \( \text{perm} \in \{ \text{RX, RWX, RWLX} \} \)
• \( (n, (\text{perm, base, end})) \in \text{executeCondition}(g)(W) \)
then
\[(n', (\text{perm}, \text{base}, \text{end})) \in \text{executeCondition}(g)(W)\]

Proof of Lemma 42. Follows easily from definition.

Lemma 43 (enterCondition monotone w.r.t \(\supseteq_{\text{pub}}\)). If

- \(W' \supseteq_{\text{pub}} W\)
- \((n, (a, \text{base}, \text{end})) \in \text{enterCondition}(g)(W)\)

then
\[(n, (a, \text{base}, \text{end})) \in \text{enterCondition}(i, g)(W')\]

Proof of Lemma 43. Follows easily from definition.

Lemma 44 (enterCondition global monotonicity w.r.t \(\supseteq_{\text{priv}}\)). If

- \(W' \supseteq_{\text{priv}} W\)
- \((n, (a, \text{base}, \text{end})) \in \text{enterCondition}(\text{GLOBAL})(W)\)

then
\[(n, (a, \text{base}, \text{end})) \in \text{enterCondition}(\text{GLOBAL})(W')\]

Proof of Lemma 44. Assume \(W_2 \supseteq_{\text{priv}} W_1\) and \((n, (a, \text{base}, \text{end})) \in \text{enterCondition}(\text{GLOBAL})(W_1)\). Now let \(W_3 \supseteq_{\text{priv}} W_2\), \(n' < n\), and show
\[(n, ((\text{RX, GLOBAL}), \text{base}, \text{end}, a)) \in \mathcal{E}(W_3)\]
by transitivity we have \(W_3 \supseteq_{\text{priv}} W_1\), so the result follows from \((n, (a, \text{base}, \text{end})) \in \text{enterCondition}(\text{GLOBAL})(W_1)\).

Lemma 45 (enterCondition downwards-closed). If

- \(n' \leq n\)
- \((n, (a, \text{base}, \text{end})) \in \text{enterCondition}(g)(W)\)

then
\[(n', (a, \text{base}, \text{end})) \in \text{enterCondition}(g)(W)\]

Proof of Lemma 45.
5.4.7 LR Sanity lemmas

Lemma 46.
\[ \forall ms, n, W = W'. \]
\[ ms : n W \land W \equiv W' \Rightarrow ms : n W' \]
\[ \square \]

Proof of Lemma 46.

Lemma 47 (Heap satisfaction downwards closure).
\[ \forall ms, n' \leq n, W. \]
\[ ms : n W \Rightarrow ms : n' W \]
\[ \square \]

Proof of Lemma 47. Let \( ms, n' \leq n \), and \( W \) be given and assume
\[ ms : n W \]
This assumption gives us \( P : \text{active}(W) \rightarrow \text{MemSegment} \) such that
1. \( ms = \bigcup_{r \in \text{active}(W)} P(r) \)
2. \[ \forall r \in \text{active}(W). \]
\[ \exists H, s. \]
\[ W(r) = (\_, s, \_ , H) \land \]
\[ (n', P(r)) \in H(s)(\xi^{-1}(W)) \]
Using \( P \) as witness, 1. is the first condition we need. Now let \( r \) be given and use 2. to get \( H \) and \( s \) such that
3. \( W(r) = (\_, s, \_ , H) \)
4. \( (n, P(r)) \in H(s)(\xi^{-1}(W)) \)
We now need to show
\[ (n', P(r)) \in H(s)(\xi^{-1}(W)) \]
which follows from 4. \( n' \leq n \), and \( H(s)(\xi^{-1}(W)) \) is a UPred(MemSegment).
\[ \square \]

Lemma 48. If
- \( ms : n W \)
- \( (n, ((\text{perm}, g), \text{base}, \text{end}, a)) \in \text{stder}(W) \)
- \( \text{base} \leq \text{end} \)
- \( \text{perm} \in \{\text{rwlx, rwl}\} \)

then
\[ g = \text{LOCAL} \]
\[ \square \]

Proof of Lemma 48. It follows as a consequence of Lemma 9. The \( n \)-equality forces the region to be temp, so for the region name to be in \( \text{localityReg}(g, W) \), the locality must be \text{LOCAL}.
\[ \square \]
5.4.8 Malloc safe to pass to adversary

**Lemma 49** (Safe values are safe to invoke.) If \((n + 1, w) \in \mathcal{V}(W)\), then \((n, \text{updatePcPerm}(w)) \in \mathcal{E}(W)\).

**Proof.**
1. Case \(w = ((\text{perm}, g), \text{base}, \text{end}, a)\) and \(\text{base} \leq a \leq \text{end}\) and \(\text{perm} \in \{\text{RX}, \text{RWX}, \text{RWLX}\}\):
   
   1.1. \((n + 1, (\text{perm}, \text{base}, \text{end})) \in \text{executeCondition}(g)(W)\).
   By: definition of \(\mathcal{V}(W)\) using the fact that \(\text{perm} \in \{\text{RX}, \text{RWX}, \text{RWLX}\}\).
   
   1.2. \((n, ((\text{perm}, g), \text{base}, \text{end}, a)) \in \mathcal{E}(W): \) By definition of \(\text{executeCondition}\) using the fact that \(\text{base} \leq a \leq \text{end}\).

2. Case \(w = ((\text{perm}, g), \text{base}, \text{end}, a)\) and \(\text{base} \leq a \leq \text{end}\) and \(\text{perm} = E:\)

   2.1. \((n + 1, (\text{base}, \text{end}, a)) \in \text{enterCondition}(g)(W)\).
   By: definition of \(\mathcal{V}(W)\) using the fact that \(\text{perm} = E\).

   2.2. \((n, ((\text{RX}, g), \text{base}, \text{end}, a)) \in \mathcal{E}(W): \) By definition of \(\text{enterCondition}\) using the fact that \(\text{base} \leq a \leq \text{end}\).

   2.3. \(\text{updatePcPerm}(w) = ((\text{RX}, g), \text{base}, \text{end}, a)\):
   By definition of \(\text{updatePcPerm}()\)

3. Otherwise: \((n, \text{updatePcPerm}(w)) \in \mathcal{E}(W)\):
   By Lemma 7.

**Lemma 50** (Malloc is safe to pass to adversary). If \(W(r) \supseteq_{\text{malloc,0}} W\), then \((n, c_{\text{malloc}}) \in \mathcal{V}(W)\) for all \(n\).

**Proof.**
1. \(c_{\text{malloc}} = ((E, \text{GLOBAL}), \text{base}, \text{end}, a)\).
   By: the malloc specification (Specification 1).

2. Suffixes: \((n, (\text{base}, \text{end}, a)) \in \text{enterCondition}(\text{GLOBAL})(W)\).
   By definition of \(\mathcal{V}(W)\).

3. Assume: \(n' < n\), \(W' \supseteq_{\text{priv}} W\).
   Suffixes: \((n', ((\text{RX}, \text{GLOBAL}), \text{base}, \text{end}, a)), (ms) \in \mathcal{O}(W')\).
   By: definition of the \text{enterCondition}

4. Assume: \(n'' \leq n', (n'', \text{reg}) \in \mathcal{R}(W'), ms :_{\text{malloc}} W'\)
   Suffixes: \((n'', (\text{reg}[pc \mapsto ((\text{RX}, \text{GLOBAL}), \text{base}, \text{end}, a)], ms)) \in \mathcal{O}(W')\)
   By: definition of \(\mathcal{E}(W')\)

5. Assume: \(i < n'', (\text{reg}[pc \mapsto ((\text{RX}, \text{GLOBAL}), \text{base}, \text{end}, a)], ms \equiv ms' \mapsto (\text{halted, mem}')\)
   Suffixes: \(\exists W'' \supseteq_{\text{priv}} W', ms', ms'. \text{mem}' = ms' \equiv ms \equiv ms_f\) and \(ms' :_{n-i} W''\)
   By: definition of \(\mathcal{O}(W')\)

6. \(W'(r) \supseteq_{\text{priv}}_{\text{malloc},0} W'\) and \(W(r) \supseteq_{\text{priv}}_{\text{malloc},0}\) using transitivity of \(\supseteq_{\text{priv}}\).

7. \(\exists P: \text{active}(W') \rightarrow \text{MemSegment} \mspace{1mu} ms :_{\text{malloc}, P} W', \text{i.e. } ms = \bigcup_{r \in \text{active}(W')} P(r)\) and \(\forall r \in \text{active}(W'), H, s, W'(r) = (\_, s, \ldots, H)\) and \((n'', P(r)) \in H(s)(\xi^{-1}(W'))\)
   By: definition of \(ms :_{\text{malloc}, P} W'\).
8. Define \( ms_{\text{frame}} = (\bigcup_{r' \in \text{active}(W'), r' \neq r} P(r')) \uplus ms_f \). Then \( ms \uplus ms_f = P(r) \uplus ms_{\text{frame}} \) and \( P(r) \vdash_{m'} W'(r). H (W'(r).s) (\xi^{-1}(W')). \) Easy from the previous point.

9. \( P(r) \vdash_{w'} W'(r). H (W'(r).s) (\xi^{-1}(W'(r))), \) i.e. \( P(r) \vdash_{w'} [r \mapsto W'(r)]. \)

   By: the malloc specification (Specification 1) from the previous point.

10. Case: \( \text{reg}(r_1) \in \mathbb{Z} \) and \( \text{reg}(r_1) \geq 0 \)

   10.1. Define size = \( \text{reg}(r_1) \)

   10.2. \( \exists \Phi' \in \text{ExecConf}, ms'_{\text{footprint}}, ms_{\text{alloc}} \in \text{MemSegment}, j \in \mathbb{N}, j > 0 \land b', e' \in \text{Addr}, t'_{\text{malloc}} \in \text{Region.} \) \( \text{reg}([pc \mapsto ((\text{RX, GLOBAL)}, \text{base, end}, a)], ms \uplus ms_f) \rightarrow_j \Phi' \) and \( \Phi'.\text{mem} = \)

   \[ ms'_{\text{footprint}} \uplus ms_{\text{alloc}} \uplus ms_{\text{frame}} \begin{array}{c} \rightarrow \quad \vdash \quad W'(r) \end{array} \]

   and \( \text{dom}(ms_{\text{alloc}}) = [b', e'] \) and \( \forall a \in [b', e'], ms_{\text{alloc}}(a) = 0 \) and \( \Phi'.\text{reg} = \Phi.\text{reg}([pc \mapsto \text{updatePcPerm}(w_{\text{ret}})][r_1 \mapsto ((\text{RX, GLOBAL}), b', e', b')] \) and size - 1 = \( e' - b' \) with \( w_{\text{ret}} = \Phi.\text{reg}(r_1). \)

   By: the malloc specification (Specification 1).

10.3. Define \( W'' = W'[r \mapsto t'_{\text{malloc}}][i \mapsto t'_{\text{malloc}}, b', e'] \) for \( i \not\in \text{dom}(W'). \) We have that \( W'' \supseteq_{\text{pub}} [r \mapsto t'_{\text{malloc}}] \) and \( W'' \supseteq_{\text{pub}} W'. \)

   By: definition of \( \supseteq_{\text{pub}} \), using the fact that \( t'_{\text{malloc}} \supseteq_{\text{pub}} W(r). \)

10.4. \( (n'', (\text{base}', \text{end}')) \in \text{readCondition}(\text{GLOBAL})(W'') \) for all \( n''. \)

   By: definition of \( \text{readCondition} \), using the region \( W''(i) \) and Lemma 21.

10.5. \( (n'', (\text{base}', \text{end}')) \in \text{writeCondition}(\text{nw}, \text{GLOBAL})(W'') \) for all \( n''. \)

   By: definition of \( \text{writeCondition} \), using the region \( W''(i) \).

10.6. \( (n'', (p, \text{base}', \text{end}')) \in \text{executeCondition}(\text{nw}, \text{GLOBAL})(W'') \) for all \( n'', p \in \{\text{RX, RX} \}; \)

   By: the definition of \( \text{executeCondition} \), \( \text{FTLR (Theorem 2)} \) using Lemmas 38, 35 and the previous two points.

10.7. \( (n'', ((\text{RX, GLOBAL}), b', e', b')) \in V(W''); \)

   By: definition of \( V(W'') \) and the above three points.

10.8. \( (n'' - j, \Phi.\text{reg}[r_1 \mapsto ((\text{RX, GLOBAL}), b', e', b')]) \in R(W''); \)

   By Lemma 26, Lemma 27, using the fact that \( W'' \supseteq_{\text{pub}} W' \) and \( (n'', \Phi.\text{reg}) \in V(W''), \) together with the previous point.

10.9. \( (n'', ms_{\text{alloc}}) \in \text{nw}, H(\text{nw}, \cdot, \cdot, b', e') \supseteq_{\text{pub}} W'' \) for any \( n''. \)

   By definition of \( \text{nw} = \text{active}(W') \), \( H(\text{nw}, \cdot, \cdot, b', e') \supseteq_{\text{pub}} W'' \) and \( \forall a \in [b', e'], ms_{\text{alloc}}(a) = 0. \)

10.10. Define \( ms' = (\bigcup_{r' \in \text{active}(W'), r' \neq r} P(r')) \uplus ms'_{\text{footprint}} \uplus ms_{\text{alloc}}. \) Then \( \Phi'.\text{mem} = \)

   \[ ms' \uplus ms_f \begin{array}{c} \rightarrow \quad \vdash \quad W'' \end{array} \]

   By the facts that \( \Phi'.\text{mem} = ms'_{\text{footprint}} \uplus ms_{\text{alloc}} \uplus ms_{\text{frame}}, ms_{\text{frame}} = (\bigcup_{r' \in \text{active}(W'), r' \neq r} P(r')) \uplus ms_f, \) the previous point, the facts that \( ms'_{\text{footprint}} \uplus ms_f \uplus ms_{\text{frame}} \uplus ms_{\text{alloc}} \uplus ms_{\text{frame}} = (\bigcup_{r' \in \text{active}(W'), r' \neq r} P(r')) \uplus ms_f, \) and \( \forall a \in [b', e'], ms_{\text{alloc}}(a) = 0. \)

10.11. \( (n'' - j + 1, w_{\text{ret}}) \in V(W''); \)

   By Lemma 24, the fact that \( W'' \supseteq_{\text{pub}} W' \), Lemma 75, and the fact that \( (n'', w_{\text{ret}}) \in V(W''), \) which follows from \( w_{\text{ret}} = \Phi.\text{reg}(r_1) \) and \( (n'', \Phi) \in R(W''). \)

10.12. \( (n'' - j, \text{updatePcPerm}(w_{\text{ret}})) \in \mathcal{E}(W''); \)

   By Lemma 49 from the previous point.
10.13. \((n'' - j, \Phi, \text{reg}[r_1 \mapsto ((\text{RWX}, \text{GLOBAL}), b', e', b')][\text{pc} \mapsto \text{updatePcPerm}(w_{reg})], ms') \in \mathcal{O}(W'')\):
By: definition of \(\mathcal{E}(W'')\), using the previous point and the facts that \((n'' - j, \Phi, \text{reg}[r_1 \mapsto ((\text{RWX}, \text{GLOBAL}), b', e', b')][\text{pc} \mapsto \text{updatePcPerm}(w_{reg})], ms') \in \mathcal{O}(W'')\), \(\mathcal{R}(W''), \) \(ms' : n'' - j W''\)

10.14. \(i > j\) and \(\Phi' \rightarrow r_i \rightarrow (\text{halted, mem'})\).
By combining \((reg[pc \mapsto ((\text{RX}, \text{GLOBAL}), base, end, a)], ms \uplus ms_f) \rightarrow i (\text{halted, mem'})\) with \((reg[pc \mapsto ((\text{RX}, \text{GLOBAL}), base, end, a)], ms \uplus ms_f) \rightarrow j \Phi'\) using Lemma.

10.15. \(\exists W'' \supseteq \text{prev } W'', ms_r, ms'' . \text{mem'} = ms'' \uplus ms_r \uplus ms_f\) and \(ms'' : n'' W''\).
By: definition of \(\mathcal{O}(W'')\) from the two previous points.

10.16. \(W'' \supseteq \text{prev } W''\).
By Lemma \(72\) using the previous point and the fact that \(W'' \supseteq \text{pub } W'\).

11. Case: \(\text{reg}(r_1) \notin \mathbb{Z} \lor \text{reg}(r_1) < 0\)

11.1. \(\exists j . (\text{reg}[pc \mapsto ((\text{RX}, \text{GLOBAL}), base, end, a)], ms \uplus ms_f) \rightarrow j \text{ failed}\)
By: the \text{malloc} specification (Specification 1).

11.2. Contradiction with \((\text{reg}[pc \mapsto ((\text{RX}, \text{GLOBAL}), base, end, a)], ms \uplus ms_f) \rightarrow i (\text{halted, mem'})\)

\[
5.4.9 \quad \text{Fundamental theorem of logical relations}
\]

\textbf{Lemma 51} (Conditions for load instruction are sufficient). \(If\)
- \(\Phi, \text{mem} : n W\)
- \(c = ((\text{perm}, g), \text{base}, \text{end}, a)\)
- \((n, c) \in \mathcal{V}(W)\)
- \(\text{readAllowed}(\text{perm})\)
- \(\text{withinBounds}(c)\)

then \((n - 1, \Phi, \text{mem}(a)) \in \mathcal{V}(W)\)

**Proof.**
1. \((n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W)\): follows by definition of \(\mathcal{V}\) from \((n, c) \in \mathcal{V}(W)\).

2. \(\exists r \in \text{localityReg}(g, W), [\text{base}', \text{end}] \supseteq [\text{base}, \text{end}]. W(r) \nsubseteq \iota_{\text{base}', \text{end}'}\).
By definition of \(\text{readCondition}(g)(W)\).

3. \(\exists P : \text{active}(W) \rightarrow \text{MemSegment}. \Phi, \text{mem} : n, P W. \) By definition of \(\Phi, \text{mem} : n W.\)

4. \(\Phi, \text{mem} = \bigcup_{r \in \text{active}(W)} P(r)\) and \(\forall r \in \text{active}(W), \exists H, s. W(r) = (\omega, s, \omega, H)\) and \(n, P(r)) \in H(s)(\xi^{-1}(W))\).
By definition of \(\Phi, \text{mem} : n, P W.\)

5. \(r \in \text{localityReg}(g, W) \subseteq \text{active}(W)\). By definition of \(\text{localityReg}(\cdot)\) and \(\text{active}(\cdot)\).

6. \(\exists H, s. W(r) = (\omega, s, \omega, H)\) and \((n, P(r)) \in H(s)(\xi^{-1}(W))\). By specializing the result from Step 4 to the \(r\) from Step 2.

7. \((n, P(r)) \in H^\text{pub}_{\text{base}', \text{end}'}(s) (\xi^{-1}(W))\).
By combining \((n, P(r)) \in H(s)(\xi^{-1}(W))\) with \(W(r) \nsubseteq \iota^\text{pub}_{\text{base}', \text{end}'}\) from Step 2.

68
Proof. By inspection of the definition of $H_{\text{base}', \text{end}'}^{\text{wul}}$.

9. $a \in [\text{base}, \text{end}] \subseteq [\text{base}', \text{end}']$. By combining withinBounds(c) with the fact that $[\text{base}', \text{end}'] \supseteq [\text{base}, \text{end}]$, from Step 2.

10. In particular, we get: $\Phi.\text{mem}(a) = P(r)(a)$ and $(n - 1, P(r)(a)) \in \mathcal{V}(W)$.

\begin{lemma}[Conditions for lea instruction are sufficient] If
\begin{itemize}
\item $(n, ((\text{perm}, g), \text{base}, \text{end}, a)) \in \mathcal{V}(W)$
\item $\text{perm} \neq \mathcal{E}$
\end{itemize}
then $(n, ((\text{perm}, g), \text{base}, \text{end}, a')) \in \mathcal{V}(W)$.
\end{lemma}

\begin{proof}
Follows by inspection of the cases in the definition of $\mathcal{V}(W)$: $a$ is ignored in all cases except where $\text{perm} = \mathcal{E}$.
\end{proof}

\begin{lemma}[pwl writecond implies nwl]
If $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\mathcal{I}_{\text{wul}}, g)(W)$ then $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\mathcal{I}_{\text{nul}}, g)(W)$.
\end{lemma}

\begin{proof}
1. $\exists r \in \text{localityReg}(g, W). \exists [\text{base}', \text{end}'] \supseteq [\text{base}, \text{end}]. W(r)^{n-1} \mathcal{I}_{\text{base}', \text{end}'}^{\text{wul}}$ and $W(r)$ is address-stratified: by definition of writeCondition.

2. Sufficient: $W(r) \supseteq \mathcal{I}_{\text{base}', \text{end}'}^{\text{wul}}$. By definition of writeCondition

3. $W(r) \supseteq \mathcal{I}_{\text{base}', \text{end}'}^{\text{wul}}$. Follows by Lemma 21.
\end{proof}

\begin{lemma}[execCond implies entryCond]
If $(n, (\text{rx}, \text{base}, \text{end})) \in \text{executeCondition}(g)(W)$ then $(n, (\text{base}, \text{end}, a)) \in \text{enterCondition}(g)(W)$.
\end{lemma}

\begin{proof}
1. Assume: $n' < n, W' \supseteq W$ where $g = \text{LOCAL} \Rightarrow \exists = \exists^{\text{pub}}$ and $g = \text{GLOBAL} \Rightarrow \exists = \exists^{\text{priv}}$

Suffices: $(n', ((\text{rx}, g), \text{base}, \text{end}, a)) \in \mathcal{E}(W')$

2. Case $a \in [\text{base}, \text{end}]$: Follows from the definition of executeCondition.

3. Case $a \not\in [\text{base}, \text{end}]$: Follows by Lemma 7.
\end{proof}

\begin{lemma}[Conditions for restrict instruction are sufficient]
If
\begin{itemize}
\item $(n, ((\text{perm}, g), \text{base}, \text{end}, a)) \in \mathcal{V}(W)$
\item $(\text{perm}', g') \subseteq (\text{perm}, g)$
\end{itemize}
then $(n, ((\text{perm}', g'), \text{base}, \text{end}, a)) \in \mathcal{V}(W)$.
\end{lemma}

\begin{proof}
By inspection of the definition of $\mathcal{V}(W)$, everything follows trivially except the following.

1. If $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\mathcal{I}_{\text{wul}}, g)(W)$ then $(n, (\text{base}, \text{end})) \in \text{writeCondition}(\mathcal{I}_{\text{nul}}, g)(W)$:

holds by lemma 55.
\end{proof}
2. If \((n, (rx, base, end)) \in \text{executeCondition}(g)(W)\) then \((n, (base, end, a)) \in \text{enterCondition}(g)(W)\).

\[\]

**Lemma 56** (Conditions for subseg instruction are sufficient). If

- \((n, ((\text{perm}, g), base, end, a)) \in \mathcal{V}(W)\)
- \(base \leq base'\)
- \(end' \leq end\)
- \(\text{perm} \neq e\)

then \(\((n, ((\text{perm}, g), base', end', a)) \in \mathcal{V}(W)\)\)

**Proof.** Follows easily from the definitions of \(\mathcal{V}(W)\), \(\text{readCondition}\), \(\text{writeCondition}\), \(\text{executeCondition}\).

\[\]

**Lemma 57** (Conditions for store instruction are sufficient). If

- \(ms = ms' \uplus ms_f\)
- \(ms' : n W\)
- \(((\text{perm}, g), base, end, a) = c\)
- \((n, c) \in \mathcal{V}(W)\)
- \(\text{writeAllowed}(\text{perm})\)
- \(\text{withinBounds}(c)\)
- \((n, w) \in \mathcal{V}(W)\)
- \(\text{if } w = ((\_, \text{local}), \_, \_, \_), \text{then } \text{perm} \in \{\text{rwLx}, \text{rwl}\}\)

then \(a \in \text{dom}(ms')\) (i.e. \(ms[a \mapsto w] = ms'[a \mapsto w] \uplus ms_f\)) and \(ms'[a \mapsto w] : n W\)

**Proof.**

1. \((n, (base, end)) \in \text{writeCondition}(\iota, g)(W)\) where \(\iota = \iota^{\text{pwl}}\) or \(\iota = \iota^{\text{nwl}}\) and \((if \ w = ((\_, \text{local}), \_, \_, \_), \text{then } \text{perm} \in \{\text{rwLx}, \text{rwl}\})\)

By definition of \(\mathcal{V}(W)\) and \(\text{writeAllowed}\), from \((n, c) \in \mathcal{V}(W)\), \(((\text{perm}, g), base, end, a) = c\) and \(\text{writeAllowed}(\text{perm})\) and the fact that \((if \ w = ((\_, \text{local}), \_, \_, \_), \text{then } \text{perm} \in \{\text{rwLx}, \text{rwl}\})\)

2. \(\exists r \in \text{localityReg}(g, W). \exists[based', end'] \supseteq [base, end]. W(r)_{n-1}^{\text{base'}, end'} \) and \(W(r)\) is address-stratified. By definition of \(\text{writeCondition}\).

3. \(\exists P : \text{active}(W) \rightarrow \text{MemSegment}. ms' : n, P W\). By definition of \(ms' : n W\).

4. \(ms' = \bigcup_{r \in \text{active}(W)} P(r)\) and \(\forall r \in \text{active}(W). \exists H, s. W(r)_{n-1}^{\text{base'}, end'} \) and \(W(r)\) is address-stratified. By definition of \(\text{writeCondition}\).

5. \(\exists H, s. W(r)_{n-1}^{\text{base'}, end'} \) and \(n, P(r) \in H(s)(\xi^{-1}(W))\). By instantiating the previous point to the \(r\) from the \(\text{writeCondition}\).
6. \((n, w) \in i. H \,(i.s) \,(\xi^{-1}(W))\) by definition of \(i^{\text{wol}}, i^{\text{nwl}}\) and the fact that \((if w = (\_ , \_ , \_ , \_ )\),
then \(i = i^{\text{wol}}\).

7. Define \(ms'_w\) such that \(\text{dom}(ms'_w) = [\text{base}', \text{end}]\), \(ms'_w(a) = w\) and \(ms'_w(a') = 0\) for \(a' \neq a\). It’s easy to show from the previous point that \((n, ms'_w) \in H(s)(\xi^{-1}(W))\).

8. \(\text{dom}(P(r)) = \text{dom}(ms'_w) = [\text{base}', \text{end}] \ni a\) and \((n, P(r)[a \mapsto w]) \in H(s)(\xi^{-1}(W))\) by applying the fact that \(W(r)\) is address-stratified, combined with the previous point.

9. Define \(P'(r) = P(r)[a \mapsto w]\) and \(P'(r') = P(r')\) for \(r' \neq r\).

10. \(ms'[a \mapsto w] = \bigcup_{r \in \text{active}(W)} P'(r)\) and \(ms'[a \mapsto w] :_{n,P} W\). By definition of \(ms'[a \mapsto w] :_{n,P} W\) and the previous two points.

\(\square\)

**Theorem 2** (Fundamental theorem of logical relations). For all \(n, \text{perm}, \text{base}, \text{end}, a, g, W\) If one of the following holds:

- \(\text{perm} = \text{RX} \land (n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W)\)

- \(\text{perm} = \text{RXX} \land (n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W) \land (n, (\text{base}, \text{end})) \in \text{writeCondition}(i^{\text{nwl}}, g)(W)\)

- \(\text{perm} = \text{RLXX} \land (n, (\text{base}, \text{end})) \in \text{readCondition}(g)(W) \land (n, (\text{base}, \text{end})) \in \text{writeCondition}(i^{\text{wol}}, g)(W)\),

then \((n, ((\text{perm}, g), \text{base}, \text{end}, a)) \in \mathcal{E}(W)\)

\(\blacksquare\)

**Proof.** 1. By induction on \(n\). In other words, assume that the theorem already holds for all \(n' < n\).

2. Assume: \(n' \leq n, (n', \text{reg}) \in \mathcal{R}(W), \text{ms} :_{n'} W\).

Suffices: \((n', \text{reg}[\text{pc} \mapsto ((\text{perm}, g), \text{base}, \text{end}, a)], \text{ms}) \in O(W)\).

By: definition of \(O(W)\).

3. Assume: \(ms_f, \text{mem}'\), \(i \leq n', \Phi = (\text{reg}[\text{pc} \mapsto ((\text{perm}, g), \text{base}, \text{end}, a)], \text{ms} \uplus ms_f)\) and \(\Phi \rightarrow_i (\text{halted}, \Phi')\).

Suffices: \(\exists W', p, W, ms_f, ms'. \Phi'.\text{mem} = ms' \uplus ms_r \uplus ms_f\) and \(ms' :_{n'-i} W'\).

By: definition of \(O(W)\)

4. \(i \neq 0\), since \((\text{reg}[\text{pc} \mapsto ((\text{perm}, g), \text{base}, \text{end}, a)], \text{ms} \uplus ms_f) \neq (\text{halted}, \Phi')\) for any \(\Phi'\).

Therefore, assume w.l.o.g. that \(i = 1 + i'\),

\[\Phi \rightarrow \text{conf'} \rightarrow_{i'} (\text{halted}, \Phi')\]
5. \( n \geq n' > 0 \), since otherwise \( i = 0 \) (because \( i \leq n' \leq n \)) and this is impossible by the previous point.

6. \((n', \Phi.\text{reg}(pc)) \in V(W)\). Proof:

6.1. Assume: \( \text{perm}' \in \{\text{RX, RWX, RWLX}\} \) with \( \text{perm}' \subseteq \text{perm} \)

Suffices: \((n', (\text{perm}', \text{base}, \text{end})) \in \text{executeCondition}(g)(W)\)

By: the definition of \( V(\cdot) \) using the assumptions

6.2. Assume: \( n'' < n', W' \supseteq W, a' \in [\text{base}, \text{end}], g = \text{LOCAL} \Rightarrow \exists = \exists^\text{pub}, g = \text{GLOBAL} \Rightarrow \exists = \exists^\text{priv} \)

Suffices: \((n'', ((\text{perm}, g), \text{base}, \text{end}, a')) \in \mathcal{E}(W')\). By: definition of \( \text{executeCondition}(g)(W) \)

6.3. By induction, using the assumptions and Lemmas 30 and 39.

7. For all \( r \in \text{RegisterName} \), \((n', \Phi.\text{reg}(r)) \in V(W)\).

7.1. Case \( r \neq pc \) follows from \((n', \text{reg}) \in R(W)\) by definition of \( R(W) \).

7.2. Case \( r = pc \): by step 6.

8. By inspection of the definitions of \( \Phi \to \text{conf}' \) and \( \lceil \text{decode}(\Phi.\text{mem}(a)) \rceil \) and \( \text{updatePcPerm}(\cdot) \) and \( \text{updatePc}(\cdot) \), it is easy to see that one of the following cases must hold:

9. Case \( \text{conf}' = \text{failed} \): contradiction, since it is not possible that \( \text{failed} \to_r \phi \) (\( \text{halted}, \Phi' \)).

10. Case \( \text{conf}' = (\text{halted}, \Phi') \):

10.1. Then \( i' = 0 \) and \( \Phi' = \Phi \)

Follows from \( (\text{halted}, \Phi) \to_r (\text{halted}, \Phi) \)

10.2. For \( W' = W, ms_r = 0 \) and \( ms' = ms \), we have that \( \Phi'.\text{mem} = \Phi'\text{mem} \uplus ms_r = ms_f \) and \( ms' = ms_r \)

using Lemma 17.

11. Case \( \text{conf}' = \Phi''[\text{reg}, pc \mapsto \text{newPc}] \), and additionally, one of the following holds:

- \( \Phi''.\text{mem} = \Phi.\text{mem} \)
- \( \Phi''.\text{mem} = \Phi.\text{mem}[a' \mapsto w] \), with \( \Phi.\text{reg}(r_1) = ((\text{perm}', g'), \text{base}', \text{end}', a') = c \) and \( \text{writeAllowed}(\text{perm}') \) and \( \text{withinBounds}(c) \) and \( w = \Phi.\text{reg}(r_2) \) and if \( w = ((\ldots, \text{LOCAL}, \ldots), \ldots) \), then \( \text{perm}' \in \{\text{RWLX, RWL}\} \)

and also one of the following holds:

- \( \text{newPc} = \text{updatePcPerm}(\Phi.\text{reg}(lv)) \)
- \( \text{newPc} = ((\text{perm}', g'), \text{base}', \text{end}', a' + 1) \) and \( \Phi''.\text{reg}(pc) = ((\text{perm}', g'), \text{base}', \text{end}', a') \)

and finally, for all \( r \in \text{RegisterName} \), one of the following holds:

- \( \Phi''.\text{reg}(r) = \Phi.\text{reg}(r) \)
- \( \Phi''.\text{reg}(r) = z \) for some \( z \in \mathbb{Z} \)
- \( \Phi''.\text{reg}(r) = w \) and \( \Phi.\text{reg}(r_2) = ((\text{perm}', g'), \text{base}', \text{end}', a') = c \) and \( \text{readAllowed}(\text{perm}') \) and \( \text{withinBounds}(c) \) and \( w = \Phi.\text{mem}(a') \)
- \( \Phi''.\text{reg}(r) = c \) and \( \Phi.\text{reg}(r_1) = ((\text{perm}', g'), \text{base}', \text{end}', a') \) and \( \text{perm}' \neq e \) and \( c = ((\text{perm}', g'), \text{base}', \text{end}', a' + z) \) for some \( z \in \mathbb{Z} \)

72
In this case, we have:

11.1. Case $\Phi' \cdot \text{mem} = ms'' \uplus ms_f$ and $ms'' :_{n'-1} W$.

11.1.1. Case $\Phi'' \cdot \text{mem} = \Phi \cdot \text{mem}$: Then $\Phi'' \cdot \text{mem} = ms \uplus ms_f$ and $ms :_{n'-1} W$ follows by Lemma 47.

11.1.2. Case $\Phi'' \cdot \text{mem} = \Phi \cdot \text{mem}(a' \mapsto w)$, with $\Phi \cdot \text{reg}(r_1) = ((\text{perm}', g'), bse', end', a') = c$ and writeAllowed(perm') and withinBounds(c) and $w = \Phi \cdot \text{reg}(r_2)$ and if $w = (\text{local}, \text{base}')$, then perm' $\in \{\text{RLX}, \text{RXL}\}$.

The facts that $\Phi'' \cdot \text{mem} = ms'' \uplus ms_f$ and $ms'' :_{n'-1} W$ follow by Lemmas 57 and 47 using the fact that $ms \uplus W$ and $(n', \Phi \cdot \text{reg}(r_1)) \in \mathcal{V}(W)$ and $(n', \Phi \cdot \text{reg}(r_2)) \in \mathcal{V}(W)$ which follows from Step 7.

11.2. For all $r \in \text{RegisterName}$. $(n'-1, \Phi'' \cdot \text{reg}(r)) \in \mathcal{V}(W)$.

11.2.1. Case $\Phi'' \cdot \text{reg}(r) = \Phi \cdot \text{reg}(r)$: $(n'-1, \Phi'' \cdot \text{reg}(r)) \in \mathcal{V}(W)$ follows from Step 7 using Lemma 75.

11.2.2. $\Phi'' \cdot \text{reg}(r) = z$ for some $z \in \mathbb{Z}$. $(n'-1, \Phi'' \cdot \text{reg}(r)) \in \mathcal{V}(W)$ follows by definition of $\mathcal{V}(\cdot)$.

11.2.3. $\Phi'' \cdot \text{reg}(r) = w$ and $\Phi \cdot \text{reg}(r_2) = ((\text{perm}', g'), bse', end', a') = c$ and readAllowed(perm') and withinBounds(c) and $w = \Phi \cdot \text{reg}(r_2)$ $\in \mathcal{V}(W)$ follows by Lemmas 51 using the fact that $\Phi \cdot \text{mem} :_{n'} W$ and $(n', \Phi \cdot \text{reg}(r_2)) \in \mathcal{V}(W)$ which we have from step 7.

11.2.4. $\Phi'' \cdot \text{reg}(r) = c$ and $\Phi \cdot \text{reg}(r_1) = ((\text{perm}', g'), bse', end', a')$ and perm' $\neq \epsilon$ and $c = ((\text{perm}', g'), bse', end', a'+z)$ for some $z \in \mathbb{Z}$: $(n'-1, \Phi'' \cdot \text{reg}(r)) \in \mathcal{V}(W)$ follows by Lemmas 52 and 75 using the fact that $(n', \Phi \cdot \text{reg}(r_1)) \in \mathcal{V}(W)$ which we have from step 7.

11.2.5. $\Phi'' \cdot \text{reg}(r) = c$ and $\Phi \cdot \text{reg}(r) = ((\text{perm}', g'), bse', end', a')$ and $(\text{perm}'', g'') \subseteq (\text{perm}', g')$ and $c = ((\text{perm}'', g''), bse', end', a')$: $(n'-1, \Phi'' \cdot \text{reg}(r)) \in \mathcal{V}(W)$ follows by Lemmas 55 and 75 using the fact that $(n', \Phi \cdot \text{reg}(r)) \in \mathcal{V}(W)$ which follows from $(n', \Phi \cdot \text{reg}) \in \mathcal{R}(W)$ by definition.

11.2.6. $\Phi'' \cdot \text{reg}(r) = c$ and $\Phi \cdot \text{reg}(r) = ((\text{perm}', g'), bse', end', a')$ and $\text{base}' \leq \text{base}''$ and $\text{end}'' \leq \text{end}'$ and $c = ((\text{perm}', g'), \text{base}'', \text{end}'', a')$ and perm' $\neq \epsilon$: $(n'-1, \Phi'' \cdot \text{reg}(r)) \in \mathcal{V}(W)$ follows by Lemmas 56 and 75 using the fact that $(n', \Phi \cdot \text{reg}(r)) \in \mathcal{V}(W)$ which follows from $(n', \Phi \cdot \text{reg}) \in \mathcal{R}(W)$ by definition.

11.3. $(n'-1, \Phi'' \cdot \text{reg}) \in \mathcal{R}(W)$: Follows from the previous point by definition of $\mathcal{R}(W)$.

11.4. $(n'-1, \text{newPc}) \in \mathcal{E}(W)$:

11.4.1. Case newPc = updatePcPerm($\Phi \cdot \text{reg}(lv)$): We distinguish the following cases:

11.4.1.1. Case $\Phi \cdot \text{reg}(lv) = ((\epsilon, g'), \text{base}', \text{end}', a')$:

11.4.1.1.1. $(n', \Phi \cdot \text{reg}(lv)) \in \mathcal{V}(W)$. Follows from Step 7.

11.4.1.1.2. $(n', (\text{base}', \text{end}', \text{adr}')) \in \text{enterCondition}(g')(W)$. By definition of $\mathcal{V}(W)$ from the previous point.

11.4.1.1.3. $(n'-1, ((\text{nx}, g'), \text{base}', \text{end}', a')) \in \mathcal{E}(W)$: By definition of enterCondition(·) and taking $n' = n'-1$ and $W' = W$.
11.4.1.4. \( \text{updatePcPerm}(\Phi \cdot \text{reg}(lv)) = ((rx, g', \text{base}', \text{end}', a')) \): by definition of \( \text{updatePcPerm}(\cdot) \).

11.4.1.2. Case \( \Phi \cdot \text{reg}(lv) = ((\text{perm}', g', \text{base}', \text{end}', a')) \) with \( \text{perm}' \in \{ \text{rx}, \text{rw}, \text{rwx}, \text{rwlx} \} \) and \( \text{withinBounds}(\Phi \cdot \text{reg}(lv)) \):

11.4.1.2.1. \( (n', \Phi \cdot \text{reg}(lv)) \in \mathcal{V}(W) \). Follows from Step 7.

11.4.1.2.2. \( (n', (\text{perm'}, g', \text{base}', \text{end}', a')) \in \text{executeCondition}(g')(W) \). By definition of \( \mathcal{V}(W) \) from the previous point.

11.4.1.2.3. \( (n' - 1, ((\text{perm}', g'), \text{base}', \text{end}', a')) \in \mathcal{E}(W) \): By definition of \( \text{executeCondition}(\cdot) \), taking \( n' = n' - 1 \), \( W' = W \) and \( a = a' \). Note that \( a' \in [\text{base}', \text{end}'] \) because we have \( \text{withinBounds}(\Phi \cdot \text{reg}(lv)) \).

11.4.1.2.4. \( \text{updatePcPerm}(\Phi \cdot \text{reg}(lv)) = ((\text{perm}', g'), \text{base}', \text{end}', a') \): by definition of \( \text{updatePcPerm}(\cdot) \).

11.4.1.3. Case not \( (\Phi \cdot \text{reg}(lv) = ((E, g'), \text{base}', \text{end}', a')) \) and not \( (\Phi \cdot \text{reg}(lv) = ((\text{perm}', g'), \text{base}', \text{end}', a')) \) with \( \text{perm}' \in \{ \text{rx}, \text{rw}, \text{rwx}, \text{rwlx} \} \) and \( \text{withinBounds}(\Phi \cdot \text{reg}(lv)) \):

11.4.1.3.1. \( \text{updatePcPerm}(\Phi \cdot \text{reg}(lv)) = \Phi \cdot \text{reg}(lv) \): by definition of \( \text{updatePcPerm}(\cdot) \).

11.4.1.3.2. \( (\text{reg}[pc \mapsto \Phi \cdot \text{reg}(lv)], \text{ms}) \rightarrow \text{failed} \) for any \( \text{reg}, \text{ms} \): by definition of the evaluation relation.

11.4.1.3.3. \( (n' - 1, \text{newPc}) \in \mathcal{E}(W) \): by Lemma 7 using the previous point.

11.4.2. Case \( \text{newPc} = ((\text{perm}', g'), \text{base}', \text{end}', a'+1) \) and \( \Phi' \cdot \text{reg}(pc) = ((\text{perm}', g'), \text{base}', \text{end}', a') \):

11.4.2.1. Case \( \text{perm}' \in \{ \text{rx}, \text{rw}, \text{rwx}, \text{rwlx} \} \) and \( \text{base}' \leq a' + 1 \leq \text{end}' \):

11.4.2.1.1. \( (n' - 1, \Phi'' \cdot \text{reg}(pc)) \in \mathcal{V}(W) \): by Step 11.2.

11.4.2.1.2. \( (n' - 1, ((\text{perm}', g'), \text{base}', \text{end}', a' + 1)) \in \mathcal{V}(W) \): by Lemma 52 from the previous point.

11.4.2.1.3. One of the following holds:

\[ perm' = \text{rx} \wedge \]
\[ (n' - 1, (\text{base}', \text{end}')) \in \text{readCondition}(g')(W) \]

\[ perm' = \text{rw} \wedge \]
\[ (n' - 1, (\text{base}', \text{end}')) \in \text{readCondition}(g')(W) \wedge \]
\[ (n' - 1, (\text{base}', \text{end}')) \in \text{writeCondition}(\text{rw}, g')(W) \]

\[ perm' = \text{rwx} \wedge \]
\[ (n' - 1, (\text{base}', \text{end}')) \in \text{readCondition}(g')(W) \wedge \]
\[ (n' - 1, (\text{base}', \text{end}')) \in \text{writeCondition}(\text{rwx}, g')(W) \],

This follows from the previous point by definition of \( \mathcal{V}(W) \).

11.4.2.1.4. \( (n' - 1, ((\text{perm}', g'), \text{base}', \text{end}', a' + 1)) \in \mathcal{E}(W) \): By the induction hypothesis of this lemma using the previous point.

11.4.2.2. Case not \( (\text{perm}' \in \{ \text{rx}, \text{rw}, \text{rwx}, \text{rwlx} \} \) and \( \text{base}' \leq a' + 1 \leq \text{end}' \): The result follows by Lemma 7.

11.5. \( (n' - 1, (\Phi'' \cdot \text{reg}[pc \mapsto \text{newPc}], \text{ms}'')) \in \mathcal{O}(W) \): by definition of \( \mathcal{E}(W) \) using the above three points.

11.6. \( \exists \text{ms}' \in \text{prms} W, \text{ms}_r, \text{ms}_f \). \( \Phi' \cdot \text{mem} = \text{ms}' \uplus \text{ms}_r \uplus \text{ms}_f \) and \( \text{ms}', \text{ms}'_s, \text{w}' \)

By: definition of \( \mathcal{O}(W) \) using the previous step and the evaluation \( \text{conf}' \rightarrow \text{halted}(\text{halted}, \Phi') \) from Step 1.
5.4.10  Scall macro-instruction correctness

**Definition 4.** We say that \((\text{reg, } ms)\) is looking at \([i_0, \cdots , i_n]\) followed by \(c_{\text{next}}\) iff

- \(\text{reg}(pc) = ((p, g), b, e, a)\)
- \(p = \text{RWX}, p = \text{RX}, \text{ or } p = \text{RWLX}\)
- \(a + n \leq e, b \leq a \leq e\)
- \(ms(a + 0, \cdots , a + n) = [i_0, \cdots , i_n]\)
- \(c_{\text{next}} = ((p, g), b, e, a + n + 1)\)

**Definition 5.** We say that \(\text{reg}\) points to stack with \(ms_{\text{stk}}\) used and \(ms_{\text{unused}}\) unused iff

- \(\text{reg}(r_{\text{stk}}) = ((\text{RWLX, LOCAL}), b_{\text{stk}}, e_{\text{stk}}, a_{\text{stk}})\)
- \(\text{dom}(ms_{\text{unused}}) = [a_{\text{stk}} + 1, \cdots , e_{\text{stk}}]\)
- \(\text{dom}(ms_{\text{stk}}) = [b_{\text{stk}}, \cdots , a_{\text{stk}}]\)
- \(b_{\text{stk}} - 1 \leq a_{\text{stk}}\)

**Lemma 58 (scall works).** If

- \(ms \vdash_n \text{revokeTemp}(W)\)
- \(\text{dom}(ms_f) \cap \text{dom}(ms_{\text{stk}} \oplus ms_{\text{unused}}) = \emptyset\)
- \((\text{reg, } ms)\) is looking at \(\text{scall} r(T_{\text{arg}}, r_{\text{priv}})\) followed by \(c_{\text{next}}\)
- \(\text{reg points to stack with } ms_{\text{stk}} \text{ used and } ms_{\text{unused}} \text{ unused}\)

**Hyp-Callee If**

- \(\text{dom}(ms_{\text{unused}}) = \text{dom}(ms_{\text{act}} \oplus ms'_{\text{unused}})\)
- \(W' = \text{revokeTemp}(W)[e_{\text{sta}}(\text{temp}, ms_{\text{stk}} \oplus ms_{\text{act}} \oplus ms_f), i_{\text{pwl}}(\text{dom}(ms'_{\text{unused}}))],\)
- \(ms'' \vdash_{n-1} W'\)
- \(\text{reg'} points to stack with } \emptyset \text{ used and } ms'_{\text{unused}} \text{ unused}\)
- \(\text{reg'} = \text{reg}\_0[p_{\text{pc}} \mapsto \text{updatePcPerm}(\text{reg}(r)), \overline{r_{\text{arg}}} \mapsto \text{reg}(\overline{r_{\text{arg}}}), r_{0} \mapsto c_{\text{ret}}, r_{\text{stk}} \mapsto c_{\text{stk}}, r \mapsto \text{reg}(r)],\)
- \((n - 1, c_{\text{ret}}) \in V(W')\)
- \((n - 1, c_{\text{stk}}) \in V(W')\)

then we have that \((n - 1, (\text{reg'}, ms'')) \in O(W')\)

**Hyp-Cont If**

- \(n' \leq n - 2\)
- \(W'' \cong^{\text{pub}} \text{revokeTemp}(W)\)
– \( ms'' \triangleright_n \text{revokeTemp}(W'') \)
– for all \( r \), we have that:

\[
\begin{align*}
\text{reg}'(r) &= c_{\text{next}} & \text{if } r = \text{pc} \\
\text{reg}'(r) &= \text{reg}(r) & \text{if } r \in r_{\text{prev}} \\
&\in \mathcal{V}(\text{revokeTemp}(W'')) & \text{if } \text{reg}'(r) \text{ is a global capability and } r \notin \{\text{pc}, r_{\text{prev}}, r_{\text{stk}}\}
\end{align*}
\]

– \( \text{reg}' \) points to stack with \( ms_{\text{stk}} \text{ used and } ms''_{\text{unused}} \text{ unused} \) for some \( ms''_{\text{unused}} \) then we have that \( (n', (\text{reg}', ms'' \uplus ms_f \uplus ms_{\text{stk}} \uplus ms''_{\text{unused}})) \in \mathcal{O}(W'') \)

Then

\[ (n, (\text{reg}, ms \uplus ms_f \uplus ms_{\text{stk}} \uplus ms_{\text{act}} \uplus ms'_{\text{unused}})) \in \mathcal{O}(W) \]

**Proof.** Assume \( n \) is sufficiently large to execute all the steps up to and including the jump of \( \text{scall } r_{\text{arg}}, r_{\text{priv}}\). If this is not the case, then in any given memory frame the execution will not halt successfully fast enough.

Further assume

1. \( ms \triangleright_n \text{revokeTemp}(W) \)
2. \( \text{dom}(ms_f) \cap (\text{dom}(ms_{\text{stk}} \uplus ms_{\text{unused}} \uplus ms)) = \emptyset \)
3. \( (\text{reg}, ms) \) is looking at \( \text{scall } r_{\text{arg}}, r_{\text{prev}}\) followed by \( c_{\text{next}} \)
4. \( \text{reg} \) points to stack with \( ms_{\text{stk}} \text{ used and } ms_{\text{unused}} \text{ unused} \)
5. Hyp-Callee
6. Hyp-Cont

Now we wish to apply Lemma. To this end let \( ms_{\text{frame}} \) be given. Executing the \( \text{scall} \) gives us

\[ (\text{reg}, ms \uplus ms_f \uplus ms_{\text{stk}} \uplus ms_{\text{act}}' \uplus ms'_{\text{unused}} \uplus ms_{\text{frame}}) \xrightarrow{i} (\text{reg}_1, ms \uplus ms_f \uplus ms_{\text{stk}} \uplus ms_{\text{act}}' \uplus ms'_{\text{unused}} \uplus ms_{\text{frame}}) \]

where

7. \( i \leq n \)
8. \( ms_{\text{act}} \) contains activation record, \( \text{reg}(r_{\text{prev}}) \), the code return capability, and the full stack capability (\( \text{reg}(r_{\text{stk}}) \) with the pointer adjusted).
9. \( \forall a \in \text{dom}(ms'_{\text{unused}}), ms'_{\text{unused}}(a) = 0 \)
10. \( \text{dom}(ms_{\text{unused}}) = \text{dom}(ms_{\text{act}} \uplus ms'_{\text{unused}}) \)
11. \( \text{reg}_1(r_0) = c_{\text{ret}} = ((E, \text{LOCAL}), \ldots, \ldots) \) where the range of authority is the same as \( \text{reg}(r_{\text{stk}}) \) and it points to the first instruction of the activation code.
12. \( \text{reg}_1 \) points to stack with \( \emptyset \) used and \( ms'_{\text{unused}} \text{ unused} \)
13. \( \text{reg}_1(\text{pc}) = \text{updatePcPerm}(\text{reg}(pc)) \)
14. \( \text{reg}_1(r) = \text{reg}(r) \)

15. \( \text{reg}_1(\overline{\text{rargs}}) = \text{reg}(\overline{\text{rargs}}) \)

16. \( \forall r' \in \text{RegisterName} \setminus \{\text{pc}, r_{\text{stk}}, \overline{\text{r}}, \overline{\text{rargs}}\}, \text{reg}_1(r') = 0 \)

In order to use Lemma \(8\), we now need to show

\[
(n_1, (\text{reg}_1, \text{ms} \uplus \text{ms}_f \uplus \text{ms}_{\text{stk}} \uplus \text{ms}_{\text{act}} \uplus \text{ms}'_{\text{unused}})) \in \mathcal{O}(W_1)
\]

where

\[
W_1 = \text{revokeTemp}(W)[\iota^{\text{sta}}(\text{temp}, \text{ms}_{\text{stk}} \uplus \text{ms}_{\text{act}} \uplus \text{ms}_f)\iota^{\text{pwl}}(\text{dom}(\text{ms}'_{\text{unused}}))]
\]

to this end use Hyp-Callee \(5.\). To use this everything is satisfied directly by assumptions but the following:

17. \( \text{ms} \uplus \text{ms}_f \uplus \text{ms}_{\text{stk}} \uplus \text{ms}_{\text{act}} \uplus \text{ms}'_{\text{unused}} \uplus n-1 W_1 \)

Here we apply Lemma \(66\). By assumption \(1\), we have \( \text{ms} : n \text{~revokeTemp}(W) \). So it suffices to show

\[
\text{ms}_f \uplus \text{ms}_{\text{stk}} \uplus \text{ms}_{\text{act}} \uplus \text{ms}'_{\text{unused}} \uplus n-1 \iota^{\text{sta}}(\text{temp}, \text{ms}_{\text{stk}} \uplus \text{ms}_{\text{act}} \uplus \text{ms}_f)\iota^{\text{pwl}}(\text{dom}(\text{ms}'_{\text{unused}}))
\]

This turns out to be trivial as \( \text{ms}_f, \text{ms}_{\text{stk}}, \) and \( \text{ms}_{\text{act}} \) match the static region. \( \text{ms}'_{\text{unused}} \) is all zeroes, to it trivially satisfies the \( \iota^{\text{pwl}} \) region.

18. \( (n-1, \text{reg}'(r_{\text{stk}})) \in \mathcal{V}(W_1) \)

Use Lemma \(62\) with \(12.\) and that \( W_1 \) has region \( \iota^{\text{pwl}}(\text{dom}(\text{ms}'_{\text{unused}})) \).

19. \( (n-1, c_{\text{ret}}) \in \mathcal{V}(W_1) \)

To this end let

19.1. \( n' < n-1 \)

19.2. \( W_2 \supseteq^{\text{pub}} W_1 \)

be given and show

\[
(n', \text{updatePcPerm}(c_{\text{ret}})) \in \mathcal{E}(W_2)
\]

To this assume

19.3. \( n'' \leq n' \)

19.4. \( (n'', \text{reg}_2) \in \mathcal{R}(W_2) \)

19.5. \( \text{ms}' : n'' W_2 \)

be given and show

\[
(n'', (\text{reg}_2[\text{pc} \mapsto \text{updatePcPerm}(c_{\text{ret}})], \text{ms}')) \in \mathcal{O}(W_2) \tag{17}
\]

From \(19.2\) and \(19.5\), we can deduce that the memory can be split in the following way:

\[
\text{ms}' = \text{ms}'' \uplus \text{ms}_r \uplus \text{ms}_{\text{stk}} \uplus \text{ms}_{\text{act}} \uplus \text{ms}'_{\text{unused}} \uplus \text{ms}_f
\]

where \( \text{ms}'' \) is the "permanent" part of memory we get from Lemma \(63\), \( \text{ms}_r \) is the part "re-voked" of memory from the same lemma that is not otherwise specified, and \( \text{dom}(\text{ms}'_{\text{unused}}) = \text{dom}(\text{ms}'_{\text{unused}}) \). From Lemma \(63\) we also get

77
19.6. \( ms'' : n'' \) `revokeTemp\( (W_2) \)

Assume \( n'' \) is large enough to execute the rest of the `call` instructions. If \( n'' \) is not large enough, then \( 17 \) is trivial to show. To show \( 17 \) apply Lemma \( 8 \) again where \( ms_r \) is the revoked part. Let \( ms'_{frame} \) be given, the execution until just after the `call` proceeds as follows:

\[
(reg_3[pc \mapsto updatePcPerm(c_{ret})], ms' \cup ms'_{var.frame}) \rightarrow j (reg_3, ms' \cup ms'_{frame})
\]

where

\[
reg_3(r) = \begin{cases} 
  c_{next} & \text{if } r = pc \\
  c_{stk} & \text{if } r = r_{stk} \\
  reg(r) & \text{if } r \in \{r_{priv}\} \\
  reg_2(r) & \text{otherwise}
\end{cases}
\]

19.7. \( reg_3 \) points to stack with \( ms_{stk} \) used and \( ms_{act} \) \( \cup ms''_{unused} \) unused

At this point, we use Hyp-Cont \( 6. \) to show the observation predicate condition of Lemma \( 8 \)

\[
(n'', (reg_3, ms'' \cup ms_{stk} \cup ms_{act} \cup ms''_{unused} \cup ms_f)) \in O(W_2)
\]

which

- \( n'' \leq n - 2 \)
  - Follows from \( 19.1 \)
- \( W_2 \trianglelefteq^{pub} revokeTemp(W) \)
  - We have

\[
W_1 \trianglelefteq^{pub} revokeTemp(W)
\]

and assumption \( 19.2 \), we get this by transitivity of \( \trianglelefteq^{pub} \).

- \( ms'' : n'' \) `revokeTemp\( (W_2) \)
  - Exactly \( 19.6 \).

  for all \( r \), we have that:

\[
reg_3(r) = \begin{cases} 
  c_{next} & \text{if } r = pc \\
  c_{stk} & \text{if } r \in r_{priv} \\
  reg(r) & \text{if } r \in V(revokeTemp(W_2)) \\
  \in V(revokeTemp(W_2)) & \text{if } reg_3(r) \text{ is a global capability and } r \in \{pc, r_{priv}, r_{stk}\}
\end{cases}
\]

The two first cases follows from \( 19.7 \). The third follow from assumption \( 19.4 \) and \( 79 \).

- \( reg' \) points to stack with \( ms_{stk} \) used and \( ms_{act} \) \( \cup ms''_{unused} \) unused
  - Exactly \( 19.8 \).
5.4.11 Malloc macro-instruction correctness

**Definition 6.** We say that 
\((reg, ms) \text{ links } key \text{ as } j \text{ to } c_{\text{malloc}}\) if \(f\)
\begin{itemize}
  \item \(reg(pc) = ((\text{perm}, g), \text{base}, \text{end}, a)\)
  \item \(ms(base) = ((\rightarrow), \text{base}_{\text{link}}, \rightarrow)\)
  \item \(ms(base_{\text{link}} + j) = c\)
\end{itemize}

**Lemma 59 (malloc works).** If
\begin{itemize}
  \item \((reg, ms)\) is looking at \texttt{malloc} \(r k\) followed by \(c_{\text{next}}\)
  \item \(k \geq 0\)
  \item \((reg, ms)\) links \texttt{malloc} as \(k\) to \(c_{\text{malloc}}\)
  \item \(c_{\text{malloc}}\) satisfies the \texttt{malloc} specification with \(\iota_{\text{malloc},0}\)
  \item \(W \supseteq \texttt{prov} [i \mapsto \iota_{\text{malloc},0}]\)
  \item \(ms : n W\)
  \item \(ms = ms' \cup ms_{\text{footprint}}\)
  \item \(ms_{\text{footprint}} : n [i \mapsto W(i)]\)
\end{itemize}

Hyp-Cont If
\begin{itemize}
  \item \(n' \leq n - 1\)
  \item \(\iota_{\text{malloc}} \supseteq \texttt{pub} W(i)\)
  \item \(ms'_{\text{footprint}} \cup ms' : n W[i \mapsto \iota_{\text{malloc}}]\)
  \item \(ms_{\text{footprint}} : n [i \mapsto W(i)]\)
  \item \(reg'(r') = \begin{cases} 
    c_{\text{next}} & r' = pc \\
    (\langle \text{RWX, GLOBAL}, \text{base}, \text{end}, a \rangle) & r' = r \\
    reg(r) & r' \notin \text{RegisterName}_1 \cup \{pc, r, r_1\} 
  \end{cases}\)
  \item \(\text{end} - \text{base} = k - 1\)
  \item \(\text{dom}(ms_{\text{alloc}}) = [\text{base}, \text{end}]\)
  \item \(\forall a \in [\text{base}, \text{end}], ms_{\text{alloc}}(a) = 0\)
\end{itemize}

Then we have \((n', (reg', ms') \cup ms'_{\text{footprint}} \cup ms_{\text{alloc}})) \in O(W[\iota_{\text{malloc}}])\)

Then
\((n, (reg, ms)) \in O(W)\)
5.4.12 Create closure macro-instruction correctness

Lemma 60 (crtcls works). If

• (reg, ms) is looking at \texttt{crtcls}(x,r) followed by \texttt{c}_{\text{next}}

• (reg, ms) links malloc as \texttt{k} to \texttt{c}_{\text{malloc}}

• \texttt{c}_{\text{malloc}} satisfies the malloc specification with \texttt{t}_{\text{malloc,0}}

• \texttt{W} \supseteq \text{prov} [i \mapsto \text{t}_{\text{malloc,0}}]

• \texttt{ms} \vdash W

• \texttt{ms} = \texttt{ms}^\prime \cup \texttt{ms}_{\text{footprint}}

• \texttt{ms}_{\text{footprint}} \vdash [i \mapsto W(i)]

\textbf{Hyp-Cont} If

\( n' \leq n \)

\( \texttt{t}_{\text{malloc}} \supseteq \text{pub} W(i) \)

\( \texttt{ms}^\prime \cup \texttt{ms}^\prime_{\text{footprint}} \vdash W [i \mapsto \text{t}_{\text{malloc}}] \)

\( \texttt{ms}^\prime_{\text{footprint}} \vdash [i \mapsto \text{t}_{\text{malloc}}] \)

\( r' = \text{pc} \)

\( r' = r_1 \)

\( r' \notin \{\text{pc, } r_1\} \cup \text{RegisterName}_i \)

\( \texttt{ms}_{\text{cls}} = \texttt{ms}_{\text{act}} \cup \texttt{ms}_{\text{env}} \)

\( \texttt{c}_{\text{cls}} = ((\text{E}, \text{GLOBAL}), \text{base}, \text{end}, \text{base} + 2) \)

\( \texttt{reg}(r) \)

\( \texttt{c}_{\text{env}} = ((\text{RW}, \text{GLOBAL}), \text{base}_{\text{env}}, \text{end}_{\text{env}}, \text{base}_{\text{env}}) \)

\( \texttt{dom}(\texttt{ms}_{\text{env}}) = [\text{base}_{\text{env}}, \text{end}_{\text{env}}] \)

\( \texttt{ms}_{\text{env}} (\text{base}_{\text{env}}, \ldots, \text{end}_{\text{env}}) = \texttt{reg}(\texttt{r}) \)

\( \texttt{Hyp-act} \)

\( \text{* } \texttt{reg}''(\texttt{pc}) = \text{updatePcPerm}(\texttt{c}_{\text{cls}}) \)

Then \( \exists k. \forall \text{ms}_f, (\texttt{reg}''', \texttt{ms}''' \cup \texttt{ms}_{\text{cls}} \cup \texttt{ms}_f) \rightarrow_k (\texttt{reg}''', \texttt{ms}'' \cup \texttt{ms}_{\text{cls}} \cup \texttt{ms}_f) \) where

\( \texttt{reg}'''(r') = \begin{cases} c_{\text{env}} & r' = c_{\text{env}} \\ \text{updatePcPerm}(\texttt{reg}(r)) & r' = \text{pc} \\ \texttt{reg}''(r') & r' \notin \text{RegisterName}_i \end{cases} \)

Then we have \((n', (\texttt{reg}', \texttt{ms}' \cup \texttt{ms}_{\text{footprint}} \cup \texttt{ms}_{\text{cls}})) \in \text{O}(W[i \mapsto \text{t}_{\text{malloc}}])\)

Then

\((n, (\text{reg}, \text{ms})) \in \text{O}(W)\)

\(\blacksquare\)
5.4.13 Helper lemmas about the stack

Lemma 61. If

• \( \text{perm} \in \{ \text{rx, rwx, rwlx} \} \)
• \( (n, (\text{base, end})) \text{readCondition} (\text{LOCAL})(W) \)
• \( (n, (\text{base, end})) \text{writeCondition} (i^{pwl}, \text{LOCAL})(W) \)

then

\[ (n, \text{perm, base, end}) \in \text{executeCondition} (\text{LOCAL})(W) \]

Proof of Lemma 61. Assume

1. \( \text{perm} \in \{ \text{rx, rwx, rwlx} \} \)
2. \( (n, (\text{base, end})) \text{readCondition} (\text{LOCAL})(W) \)
3. \( (n, (\text{base, end})) \text{writeCondition} (i^{pwl}, \text{LOCAL})(W) \)

Let \( W' \supseteq_{\text{pub}} W, a, \) and \( n' \leq n \) be given and show

\[ (n', ((\text{perm, LOCAL}), \text{base, end}, a)) \in \mathcal{E}(W') \]

Consider each of the three cases for \( \text{perm} \):

4. \( \text{perm} = \text{rwlx} \)
   In this case \( \iota = i^{pwl} \). If we use the FTLR (Theorem 2), then we are done. It suffices to show:
   
   4.1. \( (n', (\text{base, end})) \in \text{readCondition} (\text{LOCAL})(W') \)
       Follows from Lemma 34, Lemma 36 and assumption 2.
   4.2. \( (n', (\text{base, end})) \in \text{writeCondition} (i^{pwl}, \text{LOCAL})(W') \)
       Follows from Lemma 37, Lemma 36 and assumption 3.

5. \( \text{perm} = \text{rx} \)
   In this case \( \iota = i^{nwl} \). If we use the FTLR (Theorem 2), then we are done. It suffices to show:
   
   5.1. \( (n', (\text{base, end})) \in \text{readCondition} (\text{LOCAL})(W') \)
       Follows from Lemma 34, Lemma 36 and assumption 2.
   5.2. \( (n', (\text{base, end})) \in \text{writeCondition} (i^{nwl}, \text{LOCAL})(W') \)
       Follows from Lemma 33, Lemma 37, Lemma 36 and assumption 3.

6. \( \text{perm} = \text{rwx} \)
   In this case \( \iota = i^{pwl} \). If we use the FTLR (Theorem 2), then we are done. It suffices to show:
   
   6.1. \( (n', (\text{base, end})) \in \text{readCondition} (\text{LOCAL})(W') \)
       Follows from Lemma 34, Lemma 36 and assumption 2.
Lemma 62 (Stack capability in value relation). If

1. \( \text{reg} \) points to stack with \( \emptyset \) used and \( ms \) unused
2. \( \exists r. W(r) = \nu^{\text{pwl}}(\text{dom}(ms)) \)

then

\[ (n, \text{reg}(r_{stk})) \in V(W) \]

Proof of Lemma 62. Say

\( \text{reg}(r_{stk}) = c_{stk} = ((\text{rlx}, \text{local}), \text{base}, \text{end}, .) \)

Show

1. \( (n, (\text{base}, \text{end})) \in \text{readCondition}(\text{LOCAL})(W) : \)
   Amounts to \( \nu^{\text{pwl}}(\text{dom}(ms)) \subseteq \nu^{\text{pwl}}_{\text{base}, \text{end}} \)
   which is true as they are even equal.
2. \( (n, (\text{base}, \text{end})) \in \text{writeCondition}(\nu^{\text{pwl}}, \text{LOCAL})(W) : \)
   Using Lemma 12, this amounts to \( \nu^{\text{pwl}}(\text{dom}(ms)) \supseteq \nu^{\text{pwl}}_{\text{base}, \text{end}} \)
   which is true as they are even equal.
3. \( (n, (\text{rlx}, \text{base}_{stk}, \text{end}_{stk})) \in \text{executeCondition}(\text{LOCAL})(W) \)
   Using 2. and 1. we can use Lemma 61.
4. \( (n, (\text{rwx}, \text{base}_{stk}, \text{end}_{stk})) \in \text{executeCondition}(\text{LOCAL})(W) \)
   Using 2. and 1. we can use Lemma 61.
5. \( (n, (\text{rx}, \text{base}_{stk}, \text{end}_{stk})) \in \text{executeCondition}(\text{LOCAL})(W) \)
   Using 1. and 2. we can use Lemma 61.

5.4.14 Memory Segment Satisfaction

We expect the following lemmas to hold true:

Lemma 63 (Revoke temporary memory satisfaction).

\[ \forall ms, n, W, W'. \]
\[ ms : n W \Rightarrow \exists ms', ms_r. ms = ms' \uplus ms_r \land ms' : n \text{revokeTemp}(W) \]

Proof of Lemma 63.
Lemma 64 (Revoke temporary memory satisfaction 2).

\[ \forall ms, n, W, R : active(W) \rightarrow MemSegment. \]
\[ ms :_{n,p} W \Rightarrow \]
\[ \exists ms', ms_r. \]
\[ ms = ms' \uplus ms_r \land \]
\[ ms' :_{n,p|dom(W)}\text{ }revoke\text{ }Temp(W) \land \]
\[ ms_r = \biguplus_{r \in [W]_{(\text{temp})}} P(r) \land \]
\[ ms' = \biguplus_{r \in [W]_{(\text{perm})}} P(r) \]

Proof of Lemma 64.

Lemma 65 (Revoke temporary memory with stack).

\[ \forall n, ms, W, reg, stk, g, base, end, a. \]
\[ ms :_{n} W \land (n, reg) \in R(W) \land \]
\[ reg(stk) = ((\text{rwlx}, g), base, end, a) \land b \leq e \]
\[ \exists ms', ms_r. \]
\[ ms' :_{n} revoke\text{ }Temp(W) \land ms = ms' \uplus ms_r \]

Proof of Lemma 65.

Lemma 66 (Disjoint memory satisfaction).

\[ \forall n, ms, ms', ms''. \forall W, W', W''. \]
\[ ms'' = ms \uplus ms' \land W'' = W \uplus W' \land ms :_{n} W \land ms' :_{n} W' \Rightarrow \]
\[ ms'' :_{n} W'' \]

Proof of Lemma 66.

Lemma 67 (Memory satisfaction and static regions).

\[ ms :_{n} [i \mapsto \iota^{\text{sta}}(v, ms)] \]

Proof of Lemma 67.

Lemma 68 (Data only memory and standard regions). If

- \( \forall a \in \text{dom}(ms). ms(a) \in \mathbb{N} \)
- \( \iota \in \{ \iota^{\text{pwl}}, \iota^{\text{nwl}}, \iota^{\text{nwl,p}} \} \)

83
then
\[ ms : n \{ i \mapsto \iota(\text{dom}(ms)) \} \]

\hspace{1cm}

\textbf{Proof of Lemma 68.}

5.4.15 Future worlds

\textbf{Lemma 69} (World public future world of revoked world).
\[ \forall W. \text{revokeTemp}(W) \sqsupseteq \text{pub} \ W \]

\hspace{1cm}

\textbf{Proof of Lemma 69.} For all \( r \) where \( W(r) = (\text{temp}, s, \phi_{\text{pub}}, \phi, H) \), we have \( \text{revokeTemp}(W) = \) revoked. By the public future region relation we have
\[ W(r) = (\text{temp}, s, \phi_{\text{pub}}, \phi, H) \sqsupseteq \text{pub} \ \text{revokeTemp}(W)(r) = \text{revoked} \]
all other regions remain unchanged, so this follows by reflexivity of the public future region relation.

\hspace{1cm}

\textbf{Lemma 70} (World private future world of revoked world).
\[ \forall W. \text{revokeTemp}(W) \sqsupseteq \text{priv} \ W \]

\hspace{1cm}

\textbf{Proof of Lemma 70.}

\textbf{Lemma 71} (Public future world relation included in private future world relation).
\[ W' \sqsupseteq \text{pub} \ W \Rightarrow W' \sqsupseteq \text{priv} \ W \]

\hspace{1cm}

\textbf{Proof of Lemma 71.}

\textbf{Lemma 72} (Transitivity properties between private and public future worlds).
\[ W'' \sqsupseteq \text{priv} W' \land W' \sqsupseteq \text{pub} W \Rightarrow W'' \sqsupseteq \text{priv} W \]
and
\[ W'' \sqsupseteq \text{pub} W' \land W' \sqsupseteq \text{priv} W \Rightarrow W'' \sqsupseteq \text{priv} W \]

\hspace{1cm}

\textbf{Proof of Lemma 72.}

\textbf{Lemma 73.}
\[ \forall n, W_1, W_2, W'_1. \quad W_1 \equiv W_2 \land W'_1 \sqsupseteq \text{pub} W_1 \Rightarrow \exists W'_2. W'_2 \equiv W'_1 \land W'_2 \sqsupseteq \text{pub} W_2 \]

\hspace{1cm}

84
Proof of Lemma 73. Construct $W_2'$ as follows:

$$W_2(r) = \begin{cases} 
(v'_1, s'_1, \phi_{pub2}, \phi_2, H_2) & \text{if } r \in \text{dom}(W_2) \text{ and } W'_1(r) = (v'_1, s'_1, \omega, \omega) \\
W'_1(r) & \text{otherwise}
\end{cases}$$

and $W_2'(r) = (\omega, \phi_{pub2}, \phi_2, H_2)$ otherwise

Notice $\text{dom}(W'_2) = \text{dom}(W'_1)$.

Lemma 74.

$$\forall n, W_1, W_2, W'_1. \quad W_1 \equiv W_2 \land W'_1 \sqsubseteq_{priv} W_1 \Rightarrow \exists W'_2. W'_2 \equiv W'_1 \land W'_2 \sqsubseteq_{priv} W_2$$

Proof of Lemma 74. Construct $W_2'$ as follows:

$$W_2(r) = \begin{cases} 
(v'_1, s'_1, \phi_{pub2}, \phi_2, H_2) & \text{if } r \in \text{dom}(W_2) \text{ and } W'_1(r) = (v'_1, s'_1, \omega, \omega) \\
W'_1(r) & \text{otherwise}
\end{cases}$$

5.4.16 Value relation

Lemma 75 (Value relation downwards closed).

$$n' \leq n \land (n, w) \in V(W) \Rightarrow (n', w) \in V(W)$$

Proof. By definition of $V(W)$ using Lemma 36, 39, 42 and 45.

Lemma 76 (Register relation downwards closed).

$$n' \leq n \land (n, w) \in R(W) \Rightarrow (n', w) \in R(W)$$

Proof. By definition of $R(W)$ using Lemma 75.

Lemma 77 (Value relation monotone wrt $\sqsubseteq_{pub}$).

$$W' \sqsupseteq_{pub} W \land (n, w) \in V(W) \Rightarrow (n, w) \in V(W')$$

Proof of lemma 77. Follows from Lemma 34, Lemma 37, Lemma 40, and Lemma 43.

Lemma 78. If

$$(n, w) \in V(\text{revokeTemp}(W))$$

then

$$(n, w) \in V(W)$$
Proof of Lemma 78. Follows from Lemma 29, Lemma 30, Lemma 31, and Lemma 32.

Lemma 79 (Global capabilities monotone wrt $\sqsupseteq_{priv}$).

$$\forall n, perm, base, end, a, W, W'.$$

$$(n, ((perm, GLOBAL), base, end, a)) \in \mathcal{V}(W) \land W' \sqsupseteq_{priv} W$$

$$\Rightarrow (n, ((perm, GLOBAL), base, end, a)) \in \mathcal{V}(W')$$

Proof of Lemma 79. Assume

1. $perm \notin \{rwl, rwlx\}$
2. $W' \sqsupseteq_{priv} W$
3. $((n, ((perm, GLOBAL), base, end, a)) \in \mathcal{V}(W)$

and show

$$(n, ((perm, GLOBAL), base, end, a)) \in \mathcal{V}(W')$$

to this end consider the possible cases of $perm$ and show that each of the necessary conditions hold:

1. $perm = o$
   Trivial
2. $perm = ro$
   Follows from Lemma 35
3. $perm = rw$
   Follows from Lemma 35 and Lemma 38
4. $perm = rx$
   Follows from Lemma 35 and Lemma 41
5. $perm = rwx$
   Follows from Lemma 35, Lemma 38, and Lemma 41
6. $perm = e$
   Lemma 44

Lemma 80 (Non local words monotone wrt $\sqsupseteq_{priv}$).

$$\forall n, perm, base, end, a, W, W', w.$$ $w$ is non-local\)

$$(n, w) \in \mathcal{V}(W) \land W' \sqsupseteq_{priv} W$$

$$\Rightarrow (n, w) \in \mathcal{V}(W')$$

Proof of Lemma 80. If $w = ((perm, GLOBAL), base, end, a)$, then let follows from Lemma 79.

If $w \in Z$, then it follows from the fact that $i \in \mathcal{V}(W'')$ for all $i \in Z$ and $W'' \in \text{World}$. 

86
6 Other examples and applications

This section contains some ideas about other examples and applications than the ticket dispenser example.

6.1 Stack and return pointer handling without OS involvement using local capabilities

The idea of this example would be to work out and prove a calling convention that enforces well-bracketed control flow and encapsulation of local variables using CHERI’s local capabilities.

When one function invokes another function, the essential idea is that:

• Stack pointer is passed as a local and store-local capability.
• Return pointer is passed as a local capability.

Since local pointers cannot leave the registers except into regions for which a store-local capability is available, this basic idea seems to enforce a number of useful properties: well-bracketedness of control flow and encapsulation of private state stored on the stack. On the other hand, it also seems to validate the standard C treatment of the stack: the stack can be reused after a function returns, even between distrusting parties. However, safety/security of this design is very non-trivial and seems to rely on some non-trivial reasoning:

**Only stack is store-local?** A critical assumption is that adversary code has no way to store local capabilities except on the stack. The reason that it is fine to store local capabilities on the stack is that the adversary only has a local capability to the stack and cannot usefully store that capability anywhere. However, this means that we need to rely on the runtime system of our programming language to be careful when handing out store-local capabilities: only the libc startup code should initialise the stack as store-local and malloc should not produce them. This basically means that the libc initialisation code (or whatever component produces the initial stack pointer) is part of our TCB.

**Requirement for clearing the stack** Imagine the following trusted C function:

```c
void myfunction(){
    advfunction1();
    advfunction2();
}
```

where advfunction1() and advfunction2() are adversary functions. In the standard C treatment of the stack, advfunction2() would get the same stack pointer as advfunction1(). This is supposed to be safe since advfunction1() cannot have kept capabilities for the stack after its execution. But what if we require that the two functions have no way of communicating with each other? Concretely, advfunction1() has access to some secrets that must not be leaked to advfunction2(). How can we prevent advfunction1() from storing the secret somewhere on the stack and relying on advfunction2() from receiving the same stack pointer where it can read the secret? The most obvious solution seems to be that we should fully clear the stack (overwrite it with zeros) after the return of any adversary function, but this could cause an important overhead. Perhaps the processor should accommodate this with a special instruction that can zero the entire array that a capability points to?
What do return pointers look like? An important question is what return pointers look like? Since we want to protect the caller from the callee, it’s important that the return pointer is opaque, i.e. an entry pointer. The entry pointer will point to a closure that contains the next instruction to execute, as well as the previous stack pointer. But since stack pointers are local, this means that the return pointer closure should be stored in a region of memory for which we have store-local permission, i.e. on the stack. This means we need the following in our calling convention: before invoking a function, we push the stack pointer and the instruction pointer after invocation on the stack, we construct a return pointer by copying the stack pointer, limiting it to these two entries and making it an entry pointer. Then we shrink the stack pointer to the unused part of the stack and jump.

Only one-way protection in higher-order settings? Another important point is that, in a sense, local capabilities provide only one-way protection: the caller is protected from the callee but not vice-versa. Concretely: when invoking a function with some arguments marked as local, the caller is guaranteed that the callee will not have been able to store the capabilities anywhere (except perhaps on the stack, see above). However, the callee seems to have more limited guarantees: Particularly, the caller may have kept its own stack capability and this stack capability may (and typically will) also cover the part of the stack that is “owned” by the callee. In this sense, the guarantees are more limited than in a linear language.

So what does this mean? In a first-order language, this is all fine, but what if we are in a higher-order language. Imagine the following (in some ML-like language):

```haskell
let f = fun callback =>
   let ... in
   let ret = callback() in
   ...;

//adversary top function
let advtop = f( (fun y => ...) )
```

Our trusted function f is invoked by the adversary (from function advtop()) and wants to invoke an untrusted callback received from the adversary. When invoking the closure, we don’t want it to be able to access f’s local variables which it has stored on the stack. To achieve this, we only give it a stack pointer that covers the part of the stack that is unused by f. However, the callback may be implemented as an entry pointer that carries capabilities, particularly the capability to advtop’s stack pointer, which includes the part of the stack that is now used by f and contains f’s local variables.

So how do we deal with this? Perhaps we should use the fact that this is only possible when f’s callback argument is allocated to some part of the memory to which advtop has store-local permissions (since the callback contains a reference to the stack to which advtop only has a local capability). I see basically three ways to do this, all based on the idea of enforcing that the callback should be constructed in a part of memory for which no store-local permissions are available:

- One way to exclude the scenario is to require that callbacks are provided as non-local capabilities. The downside of this is that local callbacks can be useful for the caller to prevent the callee from storing them.

- Another way to exclude the scenario is to require that the stack is allocated in a fixed part of the address space and to check that callbacks point outside of this region before invoking them.
• Perhaps we should require that store-local permissions cannot be removed from a capability and simply require that callback pointers do not have store-local set. Perhaps we can allow store-local permissions to be given up, but only if the corresponding part of memory is fully zeroed in the process (or at least all local capabilities stored in the region).

6.2 A result to prove...

The simplest thing that comes to mind as a formal result for all of the above is to look at a concrete program that clearly relies on properties like well-bracketed control flow and encapsulation of local variables and prove it correct. As a concrete example: we might show an assembly program that corresponds to the following (a higher-order program that crosses trust boundaries and relies on local variable encapsulation and well-bracketed control flow):

```plaintext
let trustedCode = fun adversary =>
    let x = ref 0 in
    let callback = fun adv2 =>
        x := !x + 1;
        let y = ref (!x) in
        adv2 unit;
        assert (!x == !y);
        x := !x - 1)
    let _ = adversary callback
    assert (!x == 0)
```

7 Related reading

This is a list of related work that might be interesting to read in the context of this project.

7.1 Capability machines

7.1.1 M-Machine

More than 20 years ago, Carter et al. [1994] have described the use of capabilities in the M-Machine. They do seem to have a reference for the instruction set after all [Dally et al., 1995]; it seems like the server was just temporarily down when we were looking for this the first time...

7.1.2 CHERI

The CHERI processor is a much more recent capability machine, described by Woodruff et al. [2014], Watson et al. [2015].

Another result of this project is also CheriBSD: an adaptation of FreeBSD to the CHERI processor. It is not separately described in a published paper, but mentioned in the papers cited above and in some tech reports (see url). This work includes a pure-capability ABI that could provide some interesting examples.

The CHERI team also has a webpage with all of their CHERI-related publications (including TRs and such)

http://www.cl.cam.ac.uk/research/security/ctsrd/cheri/cheribsd.html
http://www.cl.cam.ac.uk/research/security/ctsrd/cheri/
7.2 Logical Relations

Some papers on logical relations that are relevant for this work are the following:

[Hur and Dreyer 2011] describe a logical relation between ML and a (standard) assembly language for expressing compiler correctness. Relevant because they target an assembly language, and they use biorthogonality.

[Dreyer et al. 2010] describe a logical relation for a ML-like language and use public/private transitions to reason about well-bracketed control flow. Relevant because we are considering to cover an example of enforcing well-bracketed control flow in a capability machine.

[Devriese et al. 2016] describe a logical relation for a JavaScript-like language with object capabilities. Relevant because it treats object capabilities, albeit in a JavaScript-like lambda calculus. It also deals with an untyped language, using a semantic unitype.

References


